STIC
Scientific & Technical Information Center

Search Report
EIC 3700

STIC Database Tracking Number: 244502

To: CARL ARBES
Location: RND-10A21
Art Unit: 3729
Monday, December 03, 2007

Case Serial Number: 09/888173

From: JEANNE HORRIGAN
Location: EIC3700
RND-8B31 / RND-8A34
Phone: (571)272-3529

jeanne.horrigan@uspto.gov

Search Notes

Attached are the search results for method of laying out traces on a pc board. I tagged the references that seemed most relevant to me, but I recommend that you review all of the results. In addition to bibliographic citations and abstracts, I left quite a few titles that did not seem relevant to me, but that I was unsure about.

Also attached are a copy of your search request for your files and a search feedback form (completing this is voluntary). The completed forms help ensure that our services match your needs.

EIC 3700 welcomes your feedback and would be particularly interested in knowing if you use any of these references in an office action. If you have a moment, please let us know which references you use.

I hope the results are useful. Please feel free to contact me if you have any questions or want additional searching on this application.

Jeanne Horrigan

sira
Search and Information Resources Administration

STIC Search Results Feedback Form

EIC 3700

Questions about the scope or the results of the search? Contact ***the EIC searcher or contact:***

John Sims, EIC 3700 Team Leader
RND 8B35, Phone 2-3507

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 3730*
- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
  (journal articles, conference proceedings, new product announcements etc.)

- *Relevant prior art **not found:***
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

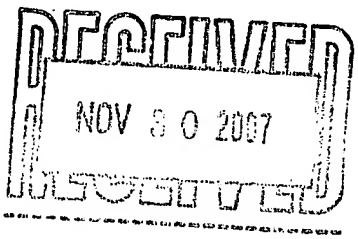
Drop off or send completed forms to STIC/EIC3700 RND 8B31

Search and Information Resources Administration

Solomon, Terrance 244502

From: CARL ARBES [carl.arbes@uspto.gov]
Sent: Thursday, November 29, 2007 6:03 PM
To: STIC-EIC3700
Subject: Database Search Request, Serial Number: 09/888,173

Requester: **CARL ARBES (P/3729)**
Art Unit: **GROUP ART UNIT 3729**
Employee Number: **59076**
Office Location: **RND 10A21**
Phone Number: **(571)272-4563**
Mailbox Number:



Case serial number: **09/888,173**
Class / Subclass(es): **29/846**
Earliest Priority Filing Date: **June 22, 2001**
Format preferred for results: **Paper**
Attachments: **No attachment.**
Search Topic Information:

method of laying out traces on a virtual printed circuit board (PcB) includes routing (or providing) a 1st trace (circuit path) on the virtual PcB, routing a 2nd trace on the virtual PcB , the 2nd trace causing crosstalk (or noise) and reducing the crosstalk between the 1st and 2nd taces by inserting a spacer between the traces.

Special Instructions and Other Comments:

p[lease use IEEE, Japio, Chinese patents, NTIS, Dissertation Abstracts, NPL and any other pertinent DBs that deal with laying out circuits onto circuit boards.

[File 2] **INSPEC** 1898-2007/Nov W3

[File 6] **NTIS** 1964-2007/Dec W3

[File 8] **Ei Compendex(R)** 1884-2007/Nov W4

[File 23] **CSA Technology Research Database** 1963-2007/Nov

[File 35] **Dissertation Abs Online** 1861-2007/Aug

[File 65] **Inside Conferences** 1993-2007/Dec 03

[File 144] **Pascal** 1973-2007/Nov W3

[File 34] **SciSearch(R) Cited Ref Sci** 1990-2007/Dec W1

[File 434] **SciSearch(R) Cited Ref Sci** 1974-1989/Dec

Set	Items	Description
S1	14	S AU=(PETUNIN V? OR PETUNIN, V?)
S2	6465	S (VIRTUAL OR DESIGN)(3N)(PCB OR CIRCUIT()BOARD? ? OR PCBS)
S3	72537	S SPACER? ?
S4	1982450	S TRACE OR TRACES OR PATH? ? OR PATHWAY? ?
S5	0	S S1 AND S2:S4
S6	12	RD S1 (unique items)
S7	**12**	**SORT S6/ALL/PY,A [not relevant]**

[File 350] **Derwent WPIX** 1963-2007/UD=200777

[File 349] **PCT FULLTEXT** 1979-2007/UB=20071122UT=20071115

[File 348] **EUROPEAN PATENTS** 1978-2007/ 200748

Set	Items	Description
S1	38	S AU=(PETUNIN V? OR PETUNIN, V?)
S2	2607	S (VIRTUAL OR DESIGN)(3N)(PCB OR CIRCUIT()BOARD? ? OR PCBS)
S3	**7**	**S S1 AND S2**
S4	220517	S SPACER? ?
S5	1222384	S TRACE OR TRACES OR PATH? ? OR PATHWAY? ?
S6	0	S (S1 AND S4) NOT S3
S7	**2**	**S (S1 AND S5) NOT S3 [1 duplicate; 1 not relevant]**

3/5/1 (Item 1 from file: 350)
Derwent WPIX

0015084097 *Drawing available*
WPI Acc no: 2005-433553/200544
Related WPI Acc No: 2003-505429; 2003-513996; 2004-832157; 2005-231380; 2005-433548
XRPX Acc No: N2005-351760
Method for integrating execution of multiple PCB application program, involves storing specific portion of generated data regarding to PCB design, in different databases associated with different applications
Patent Assignee: MENTOR GRAPHICS CORP (MENT-N)
Inventor: **PETUNIN V V**
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type

US 20050114865	A1	20050526	US 2003523697	P	20031121	200544	B
			US 2004983132	A	20041108		

Priority Applications (no., kind, date): US 2003523697 P 20031121; US 2004983132 A 20041108

Alerting Abstract US A1

NOVELTY - The method involves generating data regarding the **PCB design** in response to the predetermined input from user, and storing it in a database associated with predetermined application. Al least portion of generated data is stored in another database associated with different application. An additional data regarding the **PCB design** is generated in response to the another input using data stored in database.

DESCRIPTION - An INDEPENDENT CLAIM is also included for machine readable medium storing program for integrating execution of PCB application program.

USE - For integrating execution of several application program for designing printed circuit board (PCB) on which integrated circuits, resistor and capacitor are mounted.

ADVANTAGE - Enables to execute the several PCB application programs simultaneously in more efficient manner.

DESCRIPTION OF DRAWINGS - The figure shows the block diagram of the multiple PCB application program execution process.

5 **PCB design**

7 computer

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date			
G06F-0009/46	A	I		R	20060101			
G06F-0009/46	C	I		R	20060101			

US Classification, Issued: 719310000

DWPI Class: T01; V04

Manual Codes (EPI/S-X): T01-F02C; T01-J15A1; V04-R11

3/5/2 (Item 2 from file: 350)

Derwent WPIX

0015084092 *Drawing available*

WPI Acc no: 2005-433548/200544

Related WPI Acc No: 2003-505429; 2003-513996; 2004-832157; 2005-231380; 2005-433553

XRPX Acc No: N2005-351755

Conductive path routing method in printed circuit board design, involves assigning component pin pair to client computers that are configured to automatically route conductive paths

Patent Assignee: MENTOR GRAPHICS CORP (MENT-N)

Inventor: NATARAJAN V; **PETUNIN V V**; PFEIL C L; SMITH E F; SMITH F E; STARKOV A N; **PETUNIN V**; PFEIL C; SMITH F; STARKOV A

Patent Family (3 patents, 107 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050114821	A1	20050526	US 2003523697	P	20031121	200544	B
			US 2004870072	A	20040618		
WO 2005052730	A2	20050609	WO 2004US37183	A	20041117	200544	E
EP 1685464	A2	20060802	EP 2004800874	A	20041117	200650	E
			WO 2004US37183	A	20041117		

Priority Applications (no., kind, date): US 2003523697 P 20031121; US 2004870072 A 20040618

Alerting Abstract US A1
NOVELTY - The method involves assigning component pin pair to each client computer (5-7) configured to automatically route conductive paths between two component pins. Information related to proposed routes for conductive paths is received from each client and proposed routes are incorporated into master printed **circuit board (PCB) design** (3). Update messages indicating incorporation of the routes into **PCB design**, are forwarded to the clients.
DESCRIPTION - An INDEPENDENT CLAIM is also included for machine readable medium storing program for routing conductive paths for PCB.
USE - For conductive path routing in single/double sided printed circuit board (PCB).
ADVANTAGE - Conductive path routing for PCB can be performed automatically and quickly by using simple technique.
DESCRIPTION OF DRAWINGS - The figure shows a block diagram of computing system used in **PCB design**.
2 server
3 master **PCB design**
5-7 client computers
8 network
9 database

Class Codes
International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date			
G06F-0001/00	A	I	F	B	20060101			
G06F-0017/50	A	I		R	20060101			
G06F-0001/00	C	I	L	B	20060101			
G06F-0017/50	C	I		R	20060101			

US Classification, Issued: 716015000
DWPI Class: T01; V04
Manual Codes (EPI/S-X): T01-J15A4; T01-J16C6; T01-S03; V04-R11

3/5/3 (Item 3 from file: 350)
Derwent WPIX

0014883641 *Drawing available*
WPI Acc no: 2005-231380/200524
Related WPI Acc No: 2003-505429; 2003-513996; 2004-832157; 2005-433548; 2005-433553
XRPX Acc No: N2005-190524
Parallel printed circuit board design editing method involves displaying protective boundaries at each client while displaying sharable graphical design data and preventing each client from editing data displayed on other's boundary
Patent Assignee: MENTOR GRAPHICS CORP (MENT-N)
Inventor: **PETUNIN V V**; PFEIL C L; POTTS H; SHIKALOV V B
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050044518	A1	20050224	US 2001341037	P	20011210	200524	B
			US 2002269614	A	20021010		
			US 2003523697	P	20031121		
			US 2004780902	A	20040219		
			US 2004870497	A	20040618		

Priority Applications (no., kind, date): US 2004780902 A 20040219; US 2003523697 P 20031121; US 2002269614 A 20021010; US 2001341037 P 20011210; US 2004870497 A 20040618

Alerting Abstract US A1

NOVELTY - Protective boundaries are created and displayed at each client, while displaying the sharable graphical design data with respect to a pattern of electronic components and connections. Each client is prevented from editing the data displayed on other client's boundary.
DESCRIPTION - An INDEPENDENT CLAIM is also included for machine-readable medium storing printed **circuit board design** editing program.
USE - For simultaneous editing of parallel printed **circuit board (PCB) design**, by multiple users.
ADVANTAGE - Facilitates ease of use and conflict avoidance in a shared environment for parallel printed **circuit board design**, while preserving the integrity of the master design.
DESCRIPTION OF DRAWINGS - The figure shows a block diagram illustrating conflict prevention mechanism in parallel printed circuit board designing.
116 master design
800,802 force field width

Class Codes
International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
G06F-009/455			Main		"Version 7"

US Classification, Issued: 716011000
DWPI Class: T01; V04
Manual Codes (EPI/S-X): T01-J15A2; T01-S03; V04-Q05; V04-R11

3/5/4 (Item 4 from file: 350)
Derwent WPIX

0014650138 *Drawing available*
WPI Acc no: 2004-832157/200482
Related WPI Acc No: 2003-505429; 2003-513996; 2005-231380; 2005-433548; 2005-433553
XRPX Acc No: N2004-657556
Printed circuit board design editing method, involves allowing users to edit shared area of board design, and drawing protection border around portion of workspace, where protection border is broadcasted to other users
Patent Assignee: MENTOR GRAPHICS CORP (MENT-N)
Inventor: **PETUNIN V V**; PFEIL C L
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20040225988	A1	20041111	US 2001341037	P	20011210	200482	B
			US 2002269614	A	20021010		
			US 2003523697	P	20031121		
			US 2004780902	A	20040219		
			US 2004869923	A	20040618		

Priority Applications (no., kind, date): US 2001341037 P 20011210; US 2002269614 A 20021010; US 2003523697 P 20031121; US 2004780902 A 20040219; US 2004869923 A 20040618

Alerting Abstract US A1
NOVELTY - The method involves allowing users to edit a shared area of a printed **circuit board design**, where the users are coupled to the clients (202,204,206). A user draws a protection border around a portion of a workspace to prevent editing by other users. The border is broadcast to other users. The border defines a region in which a user makes alternative design changes without requesting corresponding changes to a master design.
DESCRIPTION - An INDEPENDENT CLAIM is also included for a machine-readable medium having stored data representing sequences of instructions which, when executed by a processor,

cause the processor to perform steps of method for editing a printed **circuit board design**.
USE - Used by an electrical engineer, for editing a printed **circuit board (PCB) design**.
ADVANTAGE - The method allows a user to simultaneously edit a **PCB design** concurrently with allowing the user to view edits to the **PCB design** by other users. The method allows the user to delineate portions of the design in which that user may experiment with various design changes before those changes are incorporated in the master printed **circuit board design**.
DESCRIPTION OF DRAWINGS - The drawing shows an entity diagram illustrating a printed **circuit board design** editing method.
200 Server
202,204,206 Clients
300 Request edit

Class Codes
International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
G06F-0017/30	A	I		R	20060101
G06F-0017/50	A	I		R	20060101
G06F-0017/30	C	I		R	20060101
G06F-0017/50	C	I		R	20060101

US Classification, Issued: 716011000, 716015000
DWPI Class: T01; V04
Manual Codes (EPI/S-X): T01-J15A2; T01-N01A2D; T01-S03; V04-R11

[File 2] **INSPEC** 1898-2007/Nov W3

[File 6] **NTIS** 1964-2007/Dec W3

[File 8] **Ei Compendex(R)** 1884-2007/Nov W4

[File 23] **CSA Technology Research Database** 1963-2007/Nov

[File 62] **SPIN(R)** 1975-2007/Nov W2

[File 144] **Pascal** 1973-2007/Nov W3

[File 95] **TEME-Technology & Management** 1989-2007/Nov W3

[File 35] **Dissertation Abs Online** 1861-2007/Aug

[File 65] **Inside Conferences** 1993-2007/Dec 03

[File 34] **SciSearch(R) Cited Ref Sci** 1990-2007/Dec W1

[File 434] **SciSearch(R) Cited Ref Sci** 1974-1989/Dec

Set	Items	Description
S1	170300	S PCB OR PCBS OR CIRCUIT()BOARD? ? OR CIRCUITBOARD? ? OR (PC OR CPU OR C()P()U OR MOTHER)()BOARD? ? OR MOTHERBOARD? ? OR CIRCUIT()CARD? ? OR PRINTED()CIRCUIT? ?
S2	5720853	S VIRTUAL OR DESIGN
S3	2804841	S TRACE OR TRACES OR PATH? ? OR PATHWAY? ? OR TRACK? ? OR CIRCUITPATH? OR ROUTE OR ROUTES OR TRAIL? ?
S4	2739585	S ROUT??? OR LAY???()OUT OR LAYOUT? ? OR PRINT??? OR CREAT??? OR ELECTROPLAT???
S5	2446751	S SPACER? ? OR BARRIER? ? OR OBSTRUCT???? OR IMPEDIMENT? OR DETERRENT? OR OBSTACLE? ? OR BLOCK???
S6	1913032	S CROSSTALK? OR CROSS()TALK? OR NOISE OR INTERFERENCE? ?
S7	1319	S S2()S1
S8	0	S S7 AND (S3(3N)S4) AND S5
S9	34729	S S3 AND S4 AND S5
S10	4	S S7 AND S9
S11	**4**	**RD (unique items)**
S12	280	S S1 AND S9
S13	26	S S6 AND S12
S14	24	S S13 NOT S10
S15	20	RD (unique items)
S16	**20**	**SORT S15/ALL/PY,A**
S17	17117	S (S4(1W)S3)(S)S5
S18	473	S (S1 OR S6) AND S17
S19	26	S (S1 AND S2) AND S17
S20	419	S S6 AND S17
S21	24	S S19 NOT (S10 OR S13)
S22	16	RD (unique items)
S23	**16**	**SORT S22/ALL/PY,A**
S24	4	S S1 AND S20
S25	0	S S24 NOT (S10 OR S13 OR S19)

11/7/1 (Item 1 from file: 2)
INSPEC

06351856 **INSPEC Abstract Number:** B9610-2210B-024, C9610-7410D-035

Title: Using interconnect synthesis technology for high speed design [PCBs]
Author Weiss, J.
Author Affiliation: Interconnectix Inc., Portland, OR, USA
Conference Title: PCB Design Conference 1996. Proceedings p. 501, 503-6
Publisher: Miller Freeman , San Francisco, CA, USA
Publication Date: 1996 **Country of Publication:** USA 576 pp.
ISBN: 0 87930 429 4 **Material Identity Number:** XX96-00396
Conference Title: Proceedings of PCB Design Conference
Conference Sponsor: Printed Circuit Design Magazine; Miller Freeman
Conference Date: 18-22 March 1996 **Conference Location:** Santa Clara, CA, USA
Language: English **Document Type:** Conference Paper (PA)
Treatment: Practical (P); Theoretical (T)
Abstract: With rise/fall time measured in picoseconds and hundreds of high-speed signal pins per design, the primary **barrier** to system speed and integrity lies in the interconnect between devices. Engineers have attempted to cope with these high-speed design challenges by utilizing complex, geometry-based design rules, followed by post-**layout** analysis to reveal inherent design flaws. As the number of high-speed pins increases, these approaches become less practical. The premise that meeting set-up and hold time requirements, clock skew management, and signal integrity specifications can be achieved by controlling **trace** length and parallelism is false. The laws of physics teach us that timing, **crosstalk**, **impedance** mismatches, and transmission line effects are not linear functions of **trace** length. This paper shows how interconnect synthesis, a high-level electrical abstraction of interconnect, generates a detailed and implementable physical representation that matches the electrical description. (0 Refs) **Subfile:** B C

11/7/2 (Item 1 from file: 8)
Ei Compendex(R)

07578235 **E.I. No:** EIP96123470774
Title: Getting systems onto printed circuit assemblies: navigating the path from concepts to successful products
Author: Seaton, John
Corporate Source: Mentor Graphics Corp, San Jose, CA, USA
Conference Title: Proceedings of the 1996 Wescon Conference
Conference Location: Anaheim, CA, USA **Conference Date:** 19961022-19961024
Sponsor: IEEE
E.I. Conference No.: 45751
Source: Wescon Conference Record 1996. Wescon, Los Angeles, CA, USA,96CH35927. p 350-356
Publication Year: 1996
CODEN: WCREDI
Language: English
Document Type: CA; (Conference Article) **Treatment:** G; (General Review)
Journal Announcement: 9702W1
Abstract: Over the years, many companies have overcome the **barriers** to successfully getting systems implemented onto **PCB** assemblies. The adoption of new **design** paradigms has solved many of the problems associated with the electrical designer making design decisions without complete information. A shift to the new paradigm has also improved the flow of market requirement and design intent information throughout the entire design process. Finally, new process management technology has greatly improved a company's ability to formally capture, distribute, and **track** their **design** processes.

11/7/3 (Item 2 from file: 8)
Fulltext available through: USPTO Full Text Retrieval Options

Ei Compendex(R)

06486517 **E.I. Monthly No:** EIM9209-045920
Title: Discrete wiring board design (CAD/CAM) for improved electrical performance.
Author: Creavin, Damien W. P.
Corporate Source: CIM Systems Technology
Conference Title: NEPCON West '92
Conference Location: Anaheim, CA, USA **Conference Date:** 19920223
E.I. Conference No.: 16594
Source: Proceedings of the Technical Program - National Electronic Packaging and Production Conference v 3. Publ by Cahner Exposition Group, Des Plaines, IL, USA. p 1123-1125
Publication Year: 1992
CODEN: NEPPAL **ISSN:** 0470-0155
Language: English
Document Type: PA; (Conference Paper) **Treatment:** A; (Applications)
Journal Announcement: 9209
Abstract: In the design of today's high speed digital systems, the interconnection techniques between devices often accounts for a majority of the overall system delay. To break through this **barrier** and to realize the true benefits of advanced IC technology, it is necessary to scale the entire interconnection system. Surface mount and TAB technology have addressed this problem at the device level; the next level of interconnection must now be addressed. This will provide high density **circuit boards** and multi-chip modules. The interconnecting **circuit board** must become an integral part of the **design** process, since many parameters must be defined other than interconnection density. Because future designs will incorporate ICs with subnanosecond rise times, power dissipation in the tens of watts, and internal propagation delays of only a few hundred picoseconds, signal **paths** must be treated as transmission lines where characteristic **impedance, crosstalk**, and propagation delay are controlled to specific values. Substrates must be capable of removing large quantities of heat while providing a controlled thermal coefficient of expansion. Microwave Board Station is a design system for high performance electronic packaging. It represents an environment within which it is possible to simultaneously manage circuits' electrical, thermal, and mechanical constraints and optimize their affects in Discrete Wiring Circuit Board manufacturing. This article discusses the Board Station environment and its PCB design tools.

11/7/4 (Item 3 from file: 8)
Ei Compendex(R)

05577156 **E.I. Monthly No:** EIM8805-024863
Title: IMPLEMENTATION ISSUES OF A TWO-LAYER BLOCK ROUTER BASED ON LEE'S ALGORITHM ON PERSONAL COMPUTERS.
Author: Srinivas, M. K.; Nandy, S. K.; Moona, Rajat
Corporate Source: Indian Inst of Science, Bangalore, India
Conference Title: Proceedings - TENCON 87: 1987 IEEE Region 10 Conference, 'Computers and Communications Technology Toward 2000'.
Conference Location: Seoul, South Korea **Conference Date:** 19870825
Sponsor: IEEE, Korea Section; IEEE, Region 10; Korea Inst of Electronic Engineers, South Korea
E.I. Conference No.: 10867
Source: Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (Cat n 87CH2423-2), Piscataway, NJ, USA p 774-778
Publication Year: 1987
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8805

Abstract: The various implementation issues of a two-layer **block router** realized on a personal computer system are addressed. The various numbering schemes used in two-dimensional and two-and-one-half dimensional implementations of the Lee algorithm are discussed. A comparative analysis is provided of three different implementations of the Lee algorithm from the point of view of constraints imposed while implementing them on the personal computer systems. A method is provided to incorporate shortest electrical connections, four **track** widths, and two pad dimensions with feedthrough minimization for two layers. 4 refs.

16/7/9 (Item 9 from file: 2)

INSPEC

08631189 **INSPEC Abstract Number:** B2003-06-2210B-002, C2003-06-7410D-070
Title: Design rules by area [PCB layout]
Author Viklund, P.
Author Affiliation: DDE USA Inc, Newport Beach, CA, USA
Journal: Printed Circuit Design vol.19, no.12 p. 12-14
Publisher: CMP Media Inc ,
Publication Date: Dec. 2002 **Country of Publication:** USA
CODEN: PCIDEU **ISSN:** 0884-9862
SICI: 0884-9862(200212)19:12L.12:DRAL;1-Z
Material Identity Number: I879-2003-001
Language: English **Document Type:** Journal Paper (JP)
Treatment: General, Review (G); Practical (P)
Abstract: New technologies often demand tighter - and more expensive requirements. One solution is to apply different rules for different regions of a design. Electrical rules ensure sufficient spacing to cope with high tension, and proper **trace** widths to cope with high currents. Electrical rules also provide for signal quality and EMC compliance. Today, some designs have 100% of their nets being constrained in these aspects. Design rules by area can be used to separate sensitive parts of a design from each other. In all simplicity, this can mean analog or digital parts, or any part of a circuit with specific requirements of some kind. It's understood that keeping function **blocks** together is a great way to battle EMI. The use of design rules by area will enable an engineer at schematic level to specify these groupings, giving valuable guidance for the design.
Subfile: B C

16/7/13 (Item 13 from file: 2)
INSPEC

09672000
Title: Suppression of parallel-plate waveguide noises excited from signal vias in multilayer boards using virtual islands
Author Seungki Nam; Yonghoon Kim; Sub Hur; Hodeok Jang; Jichai Jeong
Author Affiliation: Dept. of Radio Eng., Korea Univ., Seoul, South Korea
Conference Title: Digest. 10th International Symposium on Microwave and Optical Technology (ISMOT-2005) p. 146
Publisher: ISMOT , Japan
Publication Date: 2005 **Country of Publication:** Japan 261 pp.
ISBN: 4 9902546 0 0 **Material Identity Number:** XX-2005-01901
Conference Title: Digest. 10th International Symposium on Microwave and Optical Technology (ISMOT-2005)
Conference Date: 22-25 Aug. 2005 **Conference Location:** Fukuoka, Japan

Language: English **Document Type:** Conference Paper (PA)
Treatment: Experimental (X)
Abstract: In this paper, the mitigation method of PPW **noises** excited from signal vias in multilayer **PCBs** has been proposed. The mitigation of PPW **noises** has been achieved using the virtual islands with shorting vias. The shorting vias are used to provide the return current **path** with low **impedances** and the virtual islands are used to **block** the propagation of the PPW **noises** from the virtual islands to the rest larger **PCBs** for high frequencies. The performances of signal vias applied the virtual islands with shorting vias can be improved up to higher frequency by reducing the size of virtual islands. (2 Refs) **Subfile:** B

16/7/16 (Item 16 from file: 2)

09973436
Title: Performance analysis of signal vias using virtual islands with shorting vias in multilayer PCBs
Author Seungki Nam; Yonggyoo Kim; Yonghoon Kim; Jang, H.; Hur, S.; Song, B.; Jaehoon Lee; Jichai Jeong
Author Affiliation: Dept. of Radio Eng., Korea Univ., Seoul, South Korea
Journal: IEEE Transactions on Microwave Theory and Techniques vol.54, no.4 p. 1315-24
Publisher: IEEE ,
Publication Date: June 2006 **Country of Publication:** USA
CODEN: IETMAB **ISSN:** 0018-9480
SICI: 0018-9480(200606)54:4L.1315:PASV;1-G
Material Identity Number: I045-2006-007
Item Identifier (DOI): 10.1109/TMTT.2006.871227
Language: English **Document Type:** Journal Paper (JP)
Treatment: Theoretical (T); Experimental (X)
Abstract: The mitigation method of parallel-plate waveguide (PPW) **noises** excited from signal vias due to the mode conversion of desired propagation modes into parasitic PPW modes in multilayer **printed circuit boards** (**PCBs**) has been proposed. The mitigation of PPW **noises** has been achieved using virtual islands with shorting vias. The shorting vias are used to provide the return current **path** with low **impedances** and the virtual islands are used to **block** the propagation of the PPW noises through **PCBs**. The transmission and coupling responses of signal vias applied to the virtual islands with shorting vias are calculated using the finite-difference time-domain method to show effectiveness of the proposed mitigation method of PPW **noises**. The PPW **noises** propagating through PPWs are dramatically suppressed and the electrical performances of signal vias in multilayer **PCBs** are improved using the proposed method. The effectiveness of the proposed mitigation method of PPW **noises** is also verified by measurements of S-parameters of signal vias in simple test **boards** applied to the virtual islands with shorting vias. The effects of geometrical parameters of the virtual islands on performances of signal vias are also investigated. The performances of signal vias applied to the virtual islands with shorting vias can be improved up to higher frequency by reducing the size of virtual islands. The effect of the gapwidth of slots can be neglected. The effective number of shorting vias of the proposed mitigation method is four. Since several signal vias can be located at a virtual island, the needed number of shorting vias to obtain good transmission and coupling responses using the proposed mitigation method is less than half of that to obtain similar performance using only shorting vias. (12 Refs) **Subfile:** B

16/7/20 (Item 20 from file: 8)
Ei Compendex(R)

11926523 **E.I. No:** EIP074310879698
Title: Design of extreme connector stacking in PCI express interface
Author: Herrman, B.; Patel, P.; Mutnury, B.; Cases, M.; Pham, N.; De Araujo, D.N.
Corporate Source: IBM System and Technology Group, Research Triangle Park, NC
Conference Title: 57th Electronic Components and Technology Conference 2007, ECTC '07
Conference Location: Sparks, NV, United States **Conference Date:** 20070529-20070601
E.I. Conference No.: 70265
Source: Proceedings - Electronic Components and Technology Conference Proceedings - 57th Electronic Components and Technology Conference 2007, ECTC '07 2007.
Publication Year: 2007
CODEN: PECCA7 **ISSN:** 0569-5503 **ISBN:** 9781424409853
DOI: 10.1109/ECTC.2007.373820
DOI: 10.1109/ECTC.2007.373820
Article Number: 4249906
Language: English
Document Type: CA; (Conference Article) **Treatment:** T; (Theoretical)
Journal Announcement: 0710W4
Abstract: This paper describes the electrical architecture and design of the PCI express interface in the BladeCenter trademark left bracket 1 right bracket system. A comprehensive electrical design methodology, including accurate and detailed modeling and simulation of the complete design space, is required in order to achieve the speeds required by this interface, while using low-cost **printed circuit board** materials. In this paper, some of the **obstacles** and solutions to support 2.5 Gb/s to 5Gb/s data transmission over multiple boards and multiple connector technologies are highlighted. Pre-**layout** analysis was performed to predict the interconnect performance for relatively long **trace** lengths in FR-4 material across four connectors in order to satisfy the PCI express design requirements and guarantee the overall performance objective of the system. Signal integrity affects (including frequency dependent losses, Inter-Symbol- **Interference** (ISI), **crosstalk**, **impedance** discontinuities, via and pad capacitance effects and skew) were integrally analyzed across the complete **design** space. The solution provided was stack connector arrangements integrated into the PCI express link. The benefit was greater density, but a product that could be customized. This paper concludes the correlation between a post **route** simulation result and lab measurements. The correlation of simulation results with hardware measurements provided a high confidence in the simulation methodology, which could be relied upon in developing the broader set of **PCB** based **design** guidelines. copy 2007 IEEE. 5 Refs.

23/7/1 (Item 1 from file: 8)
Ei Compendex(R)

03906585 **E.I. Monthly No:** EI8003024173 **E.I. Yearly No:** EI80068779
Title: EVALUATION OF CONVENTIONAL AND BACKTRACKING ALGORITHMS FOR ROUTING PRINTED CIRCUIT BOARDS.
Author: Kinniment, D. J.; Weston, L. J.
Corporate Source: Univ of Manchester, Engl
Source: IEE Conference Publication n 175, Int Conf on Comput Aided Des and Manuf of Electron Components, Circ and Syst, London, Engl, Jul 3-6 1979. Publ by IEE, London, Engl, 1979 p 168-171
Publication Year: 1979
CODEN: IECPB4
Language: ENGLISH
Journal Announcement: 8003

Abstract: Hand **layout** of **printed circuit boards** has always been time consuming task; and with the increase in size and complexity of present day **PCBs** to the level where many thousands of connections sometimes need to be made on one board it has become even more difficult and tedious. The need for automation of the **routing** process has been realized for many years, and a number of algorithms have been proposed and implemented. Although many advanced **routing** algorithms have been put forward, the relative merits of the new algorithms, compared to existing methods are difficult to estimate without a direct comparison. The aim of this paper is to make such a comparison; comparing a contemporary method with one using more advanced techniques. The first method uses a fixed net ordering scheme, and a heuristic to **route** the simpler connections, followed by the well known Lee path connection algorithm for the more complex **routes**. This is compared with a method using recent developments of Lee's algorithm together with a backtracking technique in which connections may be removed and rerouted later if they **block** the path of subsequent connections. 7 refs.

23/7/2 (Item 2 from file: 2)

Fulltext available through: USPTO Full Text Retrieval Options USPTO Full Text Retrieval Options
INSPEC

03478893 **INSPEC Abstract Number:** B85040303, C85034777
Title: The benefits and trends of autorouting
Author Peddie, C.
Journal: PC Design vol.1, no.1 p. 19-20
Publication Date: Sept. 1984 **Country of Publication:** USA
CODEN: PCDEE8 **ISSN:** 8756-6311
Language: English **Document Type:** Journal Paper (JP)
Treatment: Practical (P)
Abstract: Today's **PCB** CAD system user has more control of his autorouter than ever before in that a good routing system gives him the ability to both adjust **design** rules and manipulate the **router**. He can define the **routing** process by setting such parameters as the number of passes, the amount of time spent on each **route**, the number of vias per **route**, minimum clearance, parallel line spacing, and diagonal vs. orthogonal **routing**. With each pass, or iteration, the parameters can be predefined and adjusted to follow less stringent rules. This allows the automatic **router** to follow the logical flow that a designer does when, for example, he begins his **design** with the short straight line **routes** that don't **block** channels before progressing to more complicated connections. (0 Refs)
Subfile: B C

23/7/3 (Item 3 from file: 2)
INSPEC

03636703 **INSPEC Abstract Number:** B86020916, C86020468
Title: A method for gridless routing of printed circuit boards
Author Finch, A.C.; Mackenzie, K.J.; Balsdon, G.J.; Symonds, G.
Author Affiliation: Racal-Redac Ltd., Tewkesbury, UK
Conference Title: 22nd ACM/IEEE Design Automation Conference Proceedings 1985 (Cat. No.85CH2142-8) p. 509-15
Publisher: IEEE , New York, NY, USA
Publication Date: 1985 **Country of Publication:** USA xviii+838 pp.
ISBN: 0 8186 0635 5
U.S. Copyright Clearance Center Code: 0738-100X/85/0000-0509$01.00
Conference Sponsor: IEEE; ACM
Conference Date: 23-26 June 1985 **Conference Location:** Las Vegas, NV, USA
Language: English **Document Type:** Conference Paper (PA)

Treatment: Practical (P)
Abstract: The introduction of fine-line technologies to **printed circuit board design** and manufacture has stretched most previous automatic **routing** algorithms to the limit. A different approach, designed specifically to meet the present needs, is detailed. The **router** is a single or multipass, cost-driven, multilayer, flood and backtrack type **router**. Its major difference to conventional flood type routers lies in the fact that it has no defined cell size. Each cell, or expansion area, is as large as possible. Movement from one area to another is across and 'edge' forming part of the common perimeter, or through a possible via site. Edges may also be invalid, or **blocked** edges, allowing for invalid **routes** to be found where no valid one is possible. This is utilized in the multi-pass model. The flood part of the **routing** makes no detailed decisions about **track paths,** merely defining possible **paths** in terms of abutting or overlapping expansion areas. As the areas are always rectangular, the **router** could perhaps be described as a rectangular-probe **router**. (4 Refs) **Subfile:** B C

23/7/4 (Item 4 from file: 2)

Fulltext available through: USPTO Full Text Retrieval Options USPTO Full Text Retrieval Options
INSPEC

03724303 **INSPEC Abstract Number:** B86053147, C86045402
Title: Trace routing algorithms with a PC
Author Antos, A.G.
Author Affiliation: Future Net Corp., Chatsworth, CA, USA
Journal: Printed Circuit Design vol.3, no.2 p. 11-15
Publication Date: Feb. 1986 **Country of Publication:** USA
CODEN: PCIDEU **ISSN:** 0884-9862
Language: English **Document Type:** Journal Paper (JP)
Treatment: Practical (P)
Abstract: Increasingly complex **circuit boards** for systems integrators are forcing ever greater demands on **designers**. Newer, cooler, faster CMOS devices need to be packed more tightly to yield more functionality per unit volume. Engineering changes in system peripherals can mean corresponding changes in their system interface boards, and the ability to make changes in existing board layouts its critical. Until just recently, there were only two ways to **design** the parts **layouts** and **trace routing** for system interface **boards**, either automatically on a mainframe computer, or manually. The author describes a single low cost solution to all related problems of placing electronic parts on **circuit boards** and **routing** their interconnect **trace** networks: the new generation of single-user computer-aided engineering (CAD) workstations. 'Expert' **PCB** layout software is one link in a chain of CAE tools used for product development. It is applied toward the completion of a development cycle which begins at the **block** diagram system level and ends with testing the finished **circuit boards**. Using an engineering station, computer product designers can translate system-level behavioral specifications directly into shippable, board-level products including novel system interface boards that integrate unique peripherals into new systems for untapped markets. (0 Refs) **Subfile:** B C

23/7/5 (Item 5 from file: 2)

Fulltext available through: USPTO Full Text Retrieval Options USPTO Full Text Retrieval Options
INSPEC

03974103 **INSPEC Abstract Number:** B87060538, C87055867
Title: Analogue CAE tools catching up
Author Newman, C.
Journal: New Electronics vol.20, no.11 p. 36-7
Publication Date: 26 May 1987 **Country of Publication:** UK

CODEN: NWELAC **ISSN:** 0047-9624
Language: English **Document Type:** Journal Paper (JP)
Treatment: Practical (P)
Abstract: The same **design** automation techniques being used today in the digital world apply to analogue **design**, with a few exceptions. Computer-based schematic capture tools can easily integrate analogue symbols and parts for interconnection into analogue circuits. **PCB** and semicustom layout tools can place and **route** analogue parts or functional **blocks** with the same efficiency as digital elements. (0 Refs) **Subfile:** B C

23/7/6 (Item 6 from file: 2)
Fulltext available through: USPTO Full Text Retrieval Options USPTO Full Text Retrieval Options
INSPEC

03847013 **INSPEC Abstract Number:** C87022768
Title: Better software for analog simulation
Author Carter, D.
Author Affiliation: Mentor Graphics, Beaverton, OR, USA
Journal: Computer-Aided Engineering vol.6, no.1 p. 56-7
Publication Date: Jan. 1987 **Country of Publication:** USA
CODEN: CCAEDJ **ISSN:** 0733-3536
Language: English **Document Type:** Journal Paper (JP)
Treatment: Practical (P)
Abstract: Approximately 80% of all electronic **designs** contain digital logic, so it isn't surprising that CAD tools were first developed for these applications. Automation of tasks such as schematic entry, logic simulation, and physical layout not only reduces development time but permits a greater level of **design** complexity as well. With few exceptions, the same **design** automation techniques used in the digital world apply to analog **design**. For example, computer-based schematic capture tools can easily integrate analog symbols and parts for interconnection into analog circuits. **PCB** and semicustom **layout** tools can place and **route** analog parts or functional **blocks** with the same efficiency as digital elements. Circuit simulation is one aspect of analog **design** that differs significantly from its digital counterpart, however. Successfully incorporating analog simulation into the automated **design** environment hinges on two issues: analog parts models and the efficiency of simulation in terms of both performance and the human interface. (0 Refs) **Subfile:** C

23/7/7 (Item 7 from file: 6)
Fulltext available through: Check for PDF Download Availability and Purchase
NTIS

1657343 **NTIS Accession Number:** N92-23870/8
Breathing Maze Router for Analog VLSI Cell Generation
Solel, E. ; Wimmer, S.
IBM Israel Scientific Center, Haifa.
Corporate Source Codes: 104013000; IA043855
Sponsor: National Aeronautics and Space Administration, Washington, DC.
14 Dec 89 7p
Language: English
Journal Announcement: GRAI9217; STAR3014
In Casa Ri/Sme, Proceedings of the International Conference on Cad/Cam and Amt. Volume 1: General Sessions 7 p.
NTIS Prices: (Order as N92-23851/8, PC A10/MF A03)
Country of Publication: Israel
An improvement of the maze **routing** algorithm which was developed as a part of a generator

to **design** analog VLSI (very large scale integration) CMOS (complementary metal oxide semiconductor) cells is presented. The inability of the Lee algorithm to guarantee completion and the quality of the routing, which degrades as more and more nets are being routed, have been studied in many papers. Although an impressive improvement of the original Lee algorithm has been achieved, and many layout systems employ maze routers successfully, there are inherent problems that cannot be resolved by any of the methods proposed so far. We present an algorithm that overcomes the above problems by maintaining enough room all over the maze matrix throughout the routing procedure, thus, allowing the wires to take short **routes**, without frequent **obstacle** avoidance and layer changes. This in turn reduces the number of contacts, which is an important factor in VLSI cell generation. The **virtual** area which is introduced during the **routing** procedure is eliminated later in a compaction phase, which is afforded in the environment of analog VLSI cell generation. Although it was developed for VLSI technology, the breathing algorithm is applicable to **PCB** (**printed circuit board**) **layouts**, where the location of the elements is not stiff and they can move apart.

23/7/8 (Item 8 from file: 2)

Fulltext available through: USPTO Full Text Retrieval Options USPTO Full Text Retrieval Options
INSPEC

05114487 **INSPEC Abstract Number:** B9205-2210B-001, C9205-7410D-009
Title: Routing and routers-man vs. machine?
Author Auga, K.
Author Affiliation: CAD Concepts Inc., San Jose, CA, USA
Journal: Printed Circuit Design vol.8, no.12 p. 9-11
Publication Date: Dec. 1991 **Country of Publication:** USA
CODEN: PCIDEU **ISSN:** 0884-9862
Language: English **Document Type:** Journal Paper (JP)
Treatment: Practical (P)
Abstract: Although **PCB design** involves more than just **routing traces**, this function comprises a bulk of **design** activity. Today's routers are geared toward **PCB** designers. The experienced user of a router can be almost as valuable to a company as an experienced designer or workstation user. Since writing an algorithm for every type of board is difficult, the new tools are tailored to the needs of interactive routing. The designer guides the **route** in a certain direction while the computer **routes traces** or pushes **obstacles** aside to **route** to the cursor position. Parameters that define spacing and maximum number of vias comprise interactive requirements. These types of tools are available today. Many engineers also have negative beliefs concerning the use and viability of routers. The cost of a good router is within the planned budget of most successful engineering departments. (0 Refs) **Subfile:** B C

23/7/9 (Item 9 from file: 8)
Ei Compendex(R)

06606022 **E.I. Monthly No:** EIM9305-027513
Title: Efficient routing algorithm for SOG cell generation on a dense gate-isolated layout style.
Author: Okuda, Ryosuke; Oguri, Sumio
Corporate Source: Mistubishi Electric Corp, Hyogo, Japan
Conference Title: Proceedings of the 29th ACM/IEEE Design Automation Conference
Conference Location: Anaheim, CA, USA **Conference Date:** 19920608
Sponsor: ACM SIGDA; IEEE
E.I. Conference No.: 17678
Source: Proceedings - Design Automation Conference. Publ by IEEE, IEEE Service Center,

Piscataway, NJ, USA. p 676-681
Publication Year: 1992
CODEN: PDAWDJ **ISSN:** 0146-7123 **ISBN:** 0-8186-2822-7
Language: English
Document Type: PA; (Conference Paper) **Treatment:** X; (Experimental); T; (Theoretical)
Journal Announcement: 9305
Abstract: In this paper, we propose an efficient routing algorithm for SOG cell generation on a dense gate-isolated layout style. This layout style is a difficult one for routing, because only one vertical **routing track** per one P/N pair is allowed. The key point for obtaining a complete routing is how to prevent some **routes** from **blocking** others. We propose a routing algorithm based on a simple routing model in which such a **blocking** can be easily detected and avoided in the global **routing** phase. About 87% out of 174 cells in our library has been successfully routed, which will reduce a great deal of manual efforts. (Author abstract) 11 Refs.

23/7/10 (Item 10 from file: 2)

INSPEC

05932661 **INSPEC Abstract Number:** B9506-8120J-003, C9506-7410B-015
Title: Software which automatically routes cables in a power reticulation design system
Author West, N.A.; Dwolatzky, B.; Meyer, A.S.
Author Affiliation: Dept. of Electr. Eng., Univ. of the Witwatersrand, Johannesburg, South Africa
Journal: Transactions of the South African Institute of Electrical Engineers vol.85, no.3 p. 121-30
Publication Date: Sept. 1994 **Country of Publication:** South Africa
CODEN: TSAEA9 **ISSN:** 0038-2221
Language: English **Document Type:** Journal Paper (JP)
Treatment: Practical (P)
Abstract: The subject of this paper is the development of an automatic cable **router** for use in the **design** of electricity distribution networks. Very little previous research has been done on finding optimal cable routing configurations from first principles. By "first principles", we mean that the problem is approached by considering a set of points as input and not an enumeration of all possible paths (from which an optimal solution is obtained by search). The research described in this paper approaches the problem from first principles leading to the development of two prototypes. The Lee router is based on a **printed circuit board routing** method and the Track router is based on computational geometry. Both prototypes will find the optimal **routes** between a set of points while avoiding predefined **obstacles**. The set of points represents substations, junctions and consumer connections, while the **obstacles** represent areas that the distribution cables may not cross. (13 Refs) **Subfile:** B C

23/7/11 (Item 11 from file: 2)
INSPEC

06412436 **INSPEC Abstract Number:** B9612-2210B-006, C9612-7410D-120
Title: Estimation of the number of routing layers and total wirelength in a PCB through wiring distribution analysis
Author Hom, I.; Granacki, J.
Author Affiliation: Univ. of Southern California, Marina del Rey, CA, USA
Conference Title: Proceedings EURO-DAC '96. European Design Automation Conference with EURO-VHDL '96 and Exhibition (Cat. No.96CB36000) p. 310-15

Publisher: IEEE Comput. Soc. Press , Los Alamitos, CA, USA
Publication Date: 1996 **Country of Publication:** USA xxiii+579 pp.
ISBN: 0 8186 7573 X **Material Identity Number:** XX96-03026
U.S. Copyright Clearance Center Code: 0 8186 7573 X/96/$5.00
Conference Title: Proceedings EURO-DAC '96. European Design Automation Conference with EURO-VHDL '96 and Exhibition
Conference Sponsor: Gesellschaft fur Inf. e.V.; IEEE Comput. Soc. Tech. Committee for Design Autom.; IEEE Circuits & Syst. Soc.; ACM SIGDA; IFIP 10.5; EDAC; CEPIS; Eur. C.A.D. Stand. Initiative; Osterreichische Comput. Gesellshaft; Schweizer Inf. Gesellschaft
Conference Date: 16-20 Sept. 1996 **Conference Location:** Geneva, Switzerland
Language: English **Document Type:** Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: This paper describes a model to estimate the number of **routing** layers and total wirelength for a **printed circuit board** given the netlist, partslist, placement and board form factor. The estimation model is based on analysis of the wiring distribution on the board. The wiring distribution consists of the net distribution and net segmentation. An algorithm is presented which determines the contribution of net distribution. A statistical model has been developed to estimate net segmentation as "wrong way" **routes** due to **obstacles** and congestion on a board. Routability estimations are substituted for the **routing** task while searching the **design** space, significantly reducing the **design** time since routing is the most time consuming **design** task. These estimation techniques have been successfully applied to the board estimations of several designs, including a multiprocessor **printed circuit board** and the results are presented. (8 Refs) **Subfile:** B C

23/7/12 (Item 12 from file: 8)

08219324 **E.I. No:** EIP99024553905
Title: Optimizing zig-zags in maze-routing algorithm
Author: Mani, Nallasamy; Srinivasan, Bala
Corporate Source: Monash Univ, Victoria, Aust
Conference Title: Proceedings of the 1998 IEEE International Conference on Systems, Man, and Cybernetics. Part 4 (of 5)
Conference Location: San Diego, CA, USA **Conference Date:** 19981011-19981014
Sponsor: IEEE
E.I. Conference No.: 49610
Source: Proceedings of the IEEE International Conference on Systems, Man and Cybernetics 4 1998. IEEE, Piscataway, NJ, USA,98CB36218. p 3949-3952
Publication Year: 1998
CODEN: PICYE3 **ISSN:** 1062-922X
Language: English
Document Type: CA; (Conference Article) **Treatment:** T; (Theoretical)
Journal Announcement: 9903W5
Abstract: Lee's algorithm for routing finds always a minimum length path, if one exists. We discuss an enhancement to an earlier maze-routing algorithm to reduce the number of zig-zag line segments in the **routing path**. This method would find a path between two points, if one exists, on a rectangular grid of cells. A line search method using efficient data structures has been applied that would reduce the number of line segments in the path. **Blocking** cells are introduced as **obstacles** in finding the path. All line segments are considered as horizontal and vertical only. An implementation of the method and its experimental results are reported. (Author abstract)

23/7/13 (Item 13 from file: 2)

Fulltext available through: USPTO Full Text Retrieval Options USPTO Full Text Retrieval Options
INSPEC

07144286 **INSPEC Abstract Number:** B1999-03-2210B-001, C1999-03-7410D-006
Title: A gridless line-search routing algorithm
Author Yang Rui-Yuan
Author Affiliation: Dept. of Comput., NUDT, Changsha, China
Journal: Journal of Computer Aided Design & Computer Graphics vol.10, no.3 p. 200-7
Publisher: Science Press ,
Publication Date: May 1998 **Country of Publication:** China
CODEN: JFTXFX **ISSN:** 1003-9767
SICI: 1003-9767(199805)10:3L.200:GLSR;1-M
Material Identity Number: H229-1999-003
Language: Chinese **Document Type:** Journal Paper (JP)
Treatment: Practical (P)
Abstract: Proposes an efficient and fast gridless line-search **routing** algorithm. This algorithm can be applied to connection **routing** in **printed circuit boards** (**PCBs**) and multi-chip modules (MCMs) with various pad geometries and pad sizes, with different wire widths and variable distances between wires. The **routing** efficiency is guaranteed by delicately designed data structures and by the ability to search around **obstacles**. The **routing paths** are improved by multi-phase, multi-pass refinements. The algorithm has been successfully applied in our versatile **PCB design** system "MPCB" with satisfactory results.
(5 Refs) **Subfile:** B C

23/7/14 (Item 14 from file: 2)
INSPEC

07084430 **INSPEC Abstract Number:** B9812-1130B-051, C9812-7410D-120
Title: Performance driven multi-layer general area routing for PCB/MCM designs
Author Cong, J.; Madden, P.H.
Author Affiliation: Dept. of Comput. Sci., California Univ., Los Angeles, CA, USA
Conference Title: Proceedings 1998 Design and Automation Conference. 35th DAC. (Cat. No.98CH36175) p. 356-61
Publisher: IEEE , New York, NY, USA
Publication Date: 1998 **Country of Publication:** USA xxxii+820 pp.
ISBN: 0 89791 964 5 **Material Identity Number:** XX98-02835
U.S. Copyright Clearance Center Code: 0 89791 964 5/98/06..$5.00
Conference Title: Proceedings 1998 Design and Automation Conference. 35th DAC
Conference Sponsor: ACM/SIGDA; IEEE Circuits & Syst. Soc.; EDA Consortium
Conference Date: 15-19 June 1998 **Conference Location:** San Francisco, CA, USA
Language: English **Document Type:** Conference Paper (PA)
Treatment: Practical (P)
Abstract: We present a new global **router** appropriate for Multichip Module (MCM) and dense **Printed Circuit Board** (**PCB**) **design** , which utilizes a hybrid of the classical rip-up and reroute approach, and the more recent iterative deletion method. The global router addresses performance issues by utilizing recent results in high performance interconnect **design**, while still effectively minimizing global congestion. With experiments on the maze-routing component of our global router, we show that the choice of routing cost functions can have a significant impact on final solution quality. The results of a number of previously proposed routers may be improved dramatically by adopting the cost functions we suggest here. We also find little evidence of the "net ordering problem" when our cost functions and routing model are applied. The iterative deletion method is

shown to improve global solution quality, particularly when high performance interconnect is required. We evaluate the performance of our global router by comparing the congestion of **routes** produced by our global router to those of a well known MCM router, V4R. Our global router, MINOTAUR, supports arbitrary numbers of routing layers, differing capacities for each layer, preexisting congestion and **obstacles**, and high performance interconnect structures (including those which require variable width interconnect). (
21 Refs) **Subfile:** B C

23/7/15 (Item 15 from file: 2)

INSPEC

07424668 **INSPEC Abstract Number:** B2000-01-2210B-003, C2000-01-7410D-091
Title: Re-inventing autorouters-the impact of technology evolution on PCB design
Author Pfeil, C.
Journal: Electronic Engineering vol.71, no.873 p. 87-9
Publisher: Miller Freeman ,
Publication Date: Oct. 1999 **Country of Publication:** UK
CODEN: ELCEA9 **ISSN:** 0013-4902
SICI: 0013-4902(199910)71:873L.87:IAIT;1-9
Material Identity Number: E010-1999-009
Language: English **Document Type:** Journal Paper (JP)
Treatment: General, Review (G); Practical (P)
Abstract: What makes an autorouter productive? There are many factors: speed, completion rate, high **route** quality, ability to apply and maintain high-speed rules, and the support of current packaging and fabrication technology. Yet, it is the last point that has not only been the enabler of **router** productivity, but also the reason why **routers** become extinct. Technology changes in packaging and fabrication have always kept ahead of **routing** capability. Software engineers play the game of catch-up. Their original architectures met the technology of the day, but the future will always bring unforeseen **obstacles**. If those challenges are met, the router survives. If not, the router dies. (
0 Refs) **Subfile:** B C

23/7/16 (Item 16 from file: 35)
Dissertation Abs Online

01737272 ORDER NO: AADAA-I9965895
Method of routability measure for general area routing problems
Author: Kusnadi
Degree: Ph.D.
Year: 2000
Corporate Source/Institution: The University of Arizona (0009)
Director: Jo Dale Carothers
Source: Volume 6103B of Dissertations Abstracts International.
PAGE 1553 . 105 PAGES
One of the vital phases in the **design** flow of electronic artifacts is the phase called physical **design**. In this phase -- which traditionally involves partitioning, placement and routing problems -- circuit designs are transformed into layouts ready for fabrication. Whether designing **PCBs**, MCMs or even VLSI chips, a problem that frequently arises is that of knowing if the layout will be routable. This is a classical problem of predicting routability/wireability that has been known since the early days of physical **design**. Unfortunately, quantifying the "real" routability is a difficult task and hence

the average wirelength based on the number of intramodule connections has become a common measure of routability. At the other end of this overly simplified measure, people do the actual place and **route** steps to determine the routability.

In search of a more realistic way of quantifying the routability, a new method for measuring routability/wireability is proposed for use in general area **routing** problems. It focuses on MCM and dense **PCB** designs but can be extended to any general area **routing** problem. The routability is measured by extending the counting method of Pascal's Triangle where the number of potential **routes** of each net in the **design** can be obtained precisely. The method has made it possible to evaluate the number of potential **routes** in the presence of arbitrary **obstacles** as well as the possible limitations on the number of vias/bends to use.

The theoretical development of the new method has resulted in two main algorithms called the EPTM and FEPT. Testing on several MCM benchmarks confirms what was intuitively believed that routes with 4 or less vias/bends are sufficient for general area **routing** problems in MCMs. It also uncovered the fact that increasing the number of vias/bends in the **routes** doesn't always increase the potential of routability unless detours are introduced. Further testing on non-minimum rectilinear paths shows that detours do improve the routability when the number of vias/bends between detour points is 3 or greater.

16/6/2 (Item 2 from file: 6)
Fulltext available through: Check for PDF Download Availability and Purchase
1297267 **NTIS Accession Number:** N87-18522/9
Development of an LED Display System for Cross-Track Distance and Velocity for LORAN-C Flight
Mar 87

16/6/3 (Item 3 from file: 2)
06085731 **INSPEC Abstract Number:** B9512-1210-003
Title: The decoupling of DC supply lines
Publication Date: 1994

16/6/4 (Item 4 from file: 35)
01492392 ORDER NO: AADAA-I9622938
COLLISION DETECTION FOR ROBOTICS USING DISTANCE FUNCTIONS
Year: 1995

16/6/5 (Item 5 from file: 2)
06298185 **INSPEC Abstract Number:** B9608-1220-001
Title: Tailoring feedback components prevents amplifier oscillation
Publication Date: June 1996

16/6/6 (Item 6 from file: 2)
06998583 **INSPEC Abstract Number:** B9809-2210B-007
Title: Investigation of split groundplanes at the connector for EMI control
Publication Date: 1997

16/6/8 (Item 8 from file: 144)
14713846 PASCAL No.: 00-0389384
Design of a GHz high sneed memory system
Gigahertz devices and systems : Boston MA, 20 September 1999
1999

16/6/9 (Item 9 from file: 2)
08631189 **INSPEC Abstract Number:** B2003-06-2210B-002, C2003-06-7410D-070
Title: Design rules by area [PCB layout]

Publication Date: Dec. 2002

16/6/17 (Item 17 from file: 23)
0007855038 IP Accession No: 200701-22-017311; 200701-B2-C-012976; 200701-B2-D-012976; 200701-B2-P-012976; 200701-B3-012888; 200701-B.4-012101; 200701-61-018790; 200704934
2D ultrasonic arrays with low-voltage operation for high density electronics
Publication Date: 2006

16/6/19 (Item 19 from file: 144)
17880043 PASCAL No.: 06-0480202
Multi-interval line coding technique for high speed transmissions
2006

[File 9] **Business & Industry(R)** Jul/1994-2007/Nov 26
(c) 2007 The Gale Group. All rights reserved.
[File 16] **Gale Group PROMT(R)** 1990-2007/Nov 28
(c) 2007 The Gale Group. All rights reserved.
[File 160] **Gale Group PROMT(R)** 1972-1989
(c) 1999 The Gale Group. All rights reserved.
[File 148] **Gale Group Trade & Industry DB** 1976-2007/Nov 22
(c)2007 The Gale Group. All rights reserved.
[File 621] **Gale Group New Prod.Annou.(R)** 1985-2007/Nov 23
(c) 2007 The Gale Group. All rights reserved.
[File 635] **Business Dateline(R)** 1985-2007/Dec 01
(c) 2007 ProQuest Info&Learning. All rights reserved.
[File 636] **Gale Group Newsletter DB(TM)** 1987-2007/Nov 28
(c) 2007 The Gale Group. All rights reserved.
[File 47] **Gale Group Magazine DB(TM)** 1959-2007/Nov 15
(c) 2007 The Gale group. All rights reserved.
[File 275] **Gale Group Computer DB(TM)** 1983-2007/Nov 29
(c) 2007 The Gale Group. All rights reserved.
[File 674] **Computer News Fulltext** 1989-2006/Sep W1
(c) 2006 IDG Communications. All rights reserved.
[File 647] **CMP Computer Fulltext** 1988-2007/Nov W3
(c) 2007 CMP Media, LLC. All rights reserved.
[File 624] **McGraw-Hill Publications** 1985-2007/Nov 30
(c) 2007 McGraw-Hill Co. Inc. All rights reserved.
[File 80] **TGG Aerospace/Def.Mkts(R)** 1982-2007/Nov 22
(c) 2007 The Gale Group. All rights reserved.
[File 696] **DIALOG Telecom. Newsletters** 1995-2007/Nov 30
(c) 2007 Dialog. All rights reserved.

Set	Items	Description
S1	360213	S PCB OR PCBS OR CIRCUIT()BOARD? ? OR CIRCUITBOARD? ? OR (PC OR CPU OR C()P()U OR MOTHER)()BOARD? ? OR MOTHERBOARD? ? OR CIRCUIT()CARD? ? OR PRINTED()CIRCUIT? ?
S2	5567573	S VIRTUAL OR DESIGN
S3	4040583	S TRACE OR TRACES OR PATH? ? OR PATHWAY? ? OR TRACK? ? OR CIRCUITPATH? OR ROUTE OR ROUTES OR TRAIL? ?
S4	11102190	S ROUT??? OR LAY???()OUT OR LAYOUT? ? OR PRINT??? OR CREAT??? OR ELECTROPLAT???
S5	2481114	S SPACER? ? OR BARRIER? ? OR OBSTRUCT???? OR IMPEDIMENT? OR DETERRENT? OR OBSTACLE? ? OR BLOCK???
S6	531147	S CROSSTALK? OR CROSS()TALK? OR NOISE OR INTERFERENCE? ?
S7	1104	S S2()S1
S8	26108	S (S4(3N)S3)(50N)S5
S9	3	S S7(S)S8
S10	117	S S1(S)S8
S11	10	S S6(S)S10
S12	13	S S9 OR S11
S13	9	RD (unique items)
S14	**9**	**SORT S13/ALL/PD,A**
S15	24	S S7(S)S6
S16	24	S S15 NOT S12
S17	16	RD (unique items)
S18	**16**	**SORT S17/ALL/PD,A**

14/3,K/1 (Item 1 from file: 148)
Gale Group Trade & Industry DB
(c)2007 The Gale Group. All rights reserved.
06223801 **Supplier Number:** 14409312 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Unsurpassed flexibility heralds clock generator. (Cypress Semiconductor's RoboClock)

(Cover Story)
Bursky, Dave
Electronic Design , v40 , n23 , p63(3)
Nov 12 , 1992
Document Type: Cover Story
ISSN: 0013-4872
Language: ENGLISH
Record Type: FULLTEXT; ABSTRACT
Word Count: 1325 **Line Count:** 00101
...multiple representation of the input signal.
The CY7B991 or 992 can generate clocks at a multiple of the input clock. Thus, designers are able to **route** low-frequency clock signals throughout the system and then increase their frequency at the circuit **block** of **pc board**. That helps to reduct RF **interference** genrated by the system.
The VCO is part of the PLL timing **block** that takes in the reference frequency, generates the equivalent of nearly a 1.3-Ghz signal, and delivers the desired output. Each output from the...

14/3,K/3 (Item 3 from file: 16)
Gale Group PROMT(R)

04328241 **Supplier Number:** 46344509 **(USE FORMAT 7 FOR FULLTEXT)**
Universal wiring widens LAN access at colleges
Communications News , p 28
May , 1996
Language: English **Record Type:** Fulltext
Document Type: Magazine/Journal ; Trade
Word Count: 1263
...other floor. Most of the closets contain racks of AMP 110 patch panels with RJ-45 modular jacks on the front side and 110 connector **blocks** in the rear.
'We spent a lot of time debating the merits of flying lead versus tracer-type patch panels,' says Barrett. 'In the end we picked the panels with **printed circuit traces** to connect the front and rear sides. These provide the desirable characteristics of low **crosstalk** and insertion loss for LANs.'
On the other hand, Westermeyer simply installed racks of the same modular communications outlets that reside in the user areas...

14/3,K/4 (Item 4 from file: 16)
Gale Group PROMT(R)

04669937 **Supplier Number:** 46872877 **(USE FORMAT 7 FOR FULLTEXT)**
Keeping the hot spot in IC design
Electronics Times , p 16
Nov 7 , 1996
Language: English **Record Type:** Fulltext
Document Type: Magazine/Journal ; Trade
Word Count: 863
...that Dataquest estimates as worth $263m in 1995.
With this latest acquisition, Cadence gets a technology that can wire together odd-shaped elements on a **PCB** or IC using multiple levels of wiring. What makes it important as IC process geometries shrink is that the **router** can be given rules such as the allowable **crosstalk** between wires, which it then ensures are obeyed as it **routes**. The result is

routing which takes into account deep submicron effects. Its ability to handle odd shapes also makes it useful for building large ICs out of pre-placed **blocks** borrowed from elsewhere.

Such **routers** become even more important in emerging **design** flows in which the demands of circuit timing mean synthesis has to be...

14/3,K/6 (Item 6 from file: 148)
Gale Group Trade & Industry DB

0018183948 **Supplier Number:** 131460131 (USE FORMAT 7 OR 9 FOR FULL TEXT)
All design is analog--some more so than others: digital design is becoming analog, as submicron processes require engineers to deal with the parasitic effects that result from the analog behavior of all electrical circuits.(tech trends)
Moretti, Gabe
EDN , 50 , 7 , 34(5)
March 31 , 2005
ISSN: 0012-7515
Language: English
Record Type: Fulltext
Word Count: 3421 **Line Count:** 00285
...the 1990s developed shape-based **routing**. The technique does not use an abstract grid but creates a "flood" in one direction until it reaches an **obstruction**. It then finds an unobstructed edge in the direction of the target and floods in that direction until it reaches another **obstruction**, and the process repeats until it reaches the target. The technique assesses the **route** for its length and evaluates other factors, such as parasitics, giving it significant flexibility. Because it uses real shapes of objects, designers can place **tracks** as close as possible to **obstructions**, creating a more compact **routing** pattern. And, because the net associated with each object is known, designers can apply more powerful rules to control spacing...

14/3,K/9 (Item 9 from file: 148)
Gale Group Trade & Industry DB

0018232393 **Supplier Number:** 132237442 (USE FORMAT 7 OR 9 FOR FULL TEXT)
FPGAs aid in high-end memory interface design.
Despaux, Olivier
Electronic Engineering Times , 62
May 9 , 2005
ISSN: 0192-1541
Language: English
Record Type: Fulltext
Word Count: 776 **Line Count:** 00066
...return **path** across the interface in the **pcb layout**. A discontinuity will cause the return current to take a longer **path** and will create unwanted **noise** in the system.

Olivier Despaux (olivier.despaux@xilinx.com), product applications engineer at Xilinx Inc. (San Jose)

http://www.eet.com

18/3,K/1 (Item 1 from file: 148)
Gale Group Trade & Industry DB

02835216 **Supplier Number:** 04093753 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Mechanical and electrical CAD join forces.
Rouse, Nancy E.
Machine Design , v58 , p83(5)
Jan 9 , 1986
ISSN: 0024-9114
Language: ENGLISH
Record Type: FULLTEXT
Word Count: 1522 **Line Count:** 00127
...3D modeler allows the designer to actually see components on the boards, and to interface the entire system to check if component height is causing **interference** between boards. Mechanical manipulation of boards is becoming more important as new technologies such as surface mounting, pin grid arrays, and double-sized boards increase...

18/3,K/2 (Item 2 from file: 160)
Gale Group PROMT(R)

02407707
PC-BASED PCB LAYOUT SYSTEM OUTPERFORMS WORKSTATIONS FOR FRACTION OF THE PRICE
News Release December 7, 1989 p. 1
...specially created library models. The system's extensive and flexible component library can handle digital, analogue, flexible circuit and surface mount applications and it can **design PCBs** in any shape. Multilayer **PCBs** with up to 30 physical signal layers can be designed using Ariadne 3.0 and there is a ground plane flooding capability to minimise signal **interference** problems. The system also has the ability to move any item such as copper, a line, track, component or board to any angle to give...

18/3,K/3 (Item 3 from file: 148)
Gale Group Trade & Industry DB

06393427 **Supplier Number:** 13444736 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Hot analysis tools for PCB design. (printed circuit board simulation tools that can handle thermal performance, signal integrity and electromagnetic interference)(includes related articles on board performance and on analysis sampling)
Beckert, Beverly A.
Computer-Aided Engineering , v12 , n1 , p44(4)
Jan , 1993
ISSN: 0733-3536
Language: ENGLISH
Record Type: FULLTEXT; ABSTRACT
Word Count: 3150 **Line Count:** 00265

18/3,K/4 (Item 4 from file: 148)
Gale Group Trade & Industry DB

06499883 **Supplier Number:** 14006781 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Noise vs sensitive circuits. (prevalence of noise in today's circuit designs) (includes related article on 1/f noise and directory of sources for free information on noise reduction)
Small, Charles H.

EDN , v38 , n11 , p106(8)
May 27 , 1993
ISSN: 0012-7515
Language: ENGLISH
Record Type: FULLTEXT; ABSTRACT
Word Count: 2462 **Line Count:** 00193
...for both outputs; only the final calculations and formatting differ.
PC-board layout
Designing systems that have no **noise** problems doesn't end with circuit **design**; **pc-board layout** is an important part of any analog, high-speed digital, or mixed-signal **design**. Good **pc-board layout** for **noise**-sensitive circuits begins at the prototype stage. You must pay just as much attention to supply decoupling, component placement, and signal runs in your prototype...

18/3,K/5 (Item 5 from file: 148)
Gale Group Trade & Industry DB

06785970 **Supplier Number:** 14520965 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Noise vs sensitive circuits. (EDN Technology Supplement: The Art of Noise)
Small, Charles
Electronics Weekly , n1651 , p22(3)
Sept 15 , 1993
ISSN: 0013-5224
Language: ENGLISH
Record Type: FULLTEXT; ABSTRACT
Word Count: 1840 **Line Count:** 00148
...calculator' window of Cadence's Analog Artist will yield a noise-figure plot.
Designing systems that have no **noise** problems doesn't end with circuit **design**; **PCB** layout is an important part of any analogue, high-speed digital, or mixed-signal design. Good PCB layout for **noise**-sensitive circuits begins at the prototype stage. As much attention must be paid to supply decoupling, component placement, and signal runs in the prototype as...

18/3,K/15 (Item 15 from file: 148)
Gale Group Trade & Industry DB

0018371336 **Supplier Number:** 133139000 (USE FORMAT 7 OR 9 FOR FULL TEXT)
PCI express and ASI: avoiding chaos at 2 Gbps: at data rates as high as 2 Gbps per lane, little things can make big differences in signal integrity. Experts disagree on whether thinking about what's really going on can improve performance or only make it worse.(tech trends)(Peripheral component interconnect)(Advanced Switching Interconnect)
Strassberg, Dan
EDN , 50 , 11 , 31(5)
May 26 , 2005
ISSN: 0012-7515
Language: English
Record Type: Fulltext
Word Count: 3295 **Line Count:** 00280
...fatal. Still, discontinuities and reflections in transmission paths can and do cause errors, so you must **design pc boards**, connectors, backplanes, and cables to minimize **crosstalk** and to maintain a constant-impedance environment with minimal discontinuities, and you must

also minimize delay differences that cause skew between signals that are supposed...

18/7/6 (Item 6 from file: 16)
Gale Group PROMT(R)

04663643 **Supplier Number:** 46863337 **(THIS IS THE FULLTEXT)**
VeriBest VB97
Electronic News (1991) , p 044
Nov 4 , 1996
Text:
Out of Boulder, Colo., VeriBest shipped its first software release since its spinoff from Intergraph earlier this year. VB97 contains new simulation and **printed circuit board design** (**PCB**) technologies including three new simulators; VeriBest VHDL, VeriBest Analog, and VeriBest PCB Signal Analyzer, a new signal integrity analysis tool for high speed **PCB design** addressing critical timing issues. VB97 is distributed via CD and documentation is now on-line in HTML and PDF formats. VeriBest VHDL gives a choice of hardware description languages within the VeriBest design process. The VeriBest Analog simulator has a new user interface for improved capacity and performance. The PCB Signal Analyzer provides transmission line simulation including **crosstalk** analysis using IBIS models. The waveform display tool, WaveScope, emulates a virtual oscilloscope during physical design. VeriBest VHDL and Analog are priced at $10,000 each for a floating network license on Windows NT, with the PCB Signal Analyzer priced at$15,000. All three products are available now.

[File 20] **Dialog Global Reporter** 1997-2007/Dec 03

Set Items Description
S1 66551 S PCB OR PCBS OR CIRCUIT()BOARD? ? OR CIRCUITBOARD? ? OR (PC OR CPU OR C()P()U OR MOTHER)()BOARD? ? OR MOTHERBOARD? ? OR CIRCUIT()CARD? ? OR PRINTED()CIRCUIT? ?
S2 1825311 S VIRTUAL OR DESIGN
S3 3681010 S TRACE OR TRACES OR PATH? ? OR PATHWAY? ? OR TRACK? ? OR CIRCUITPATH? OR ROUTE OR ROUTES OR TRAIL? ?
S4 7246067 S ROUT??? OR LAY???()OUT OR LAYOUT? ? OR PRINT??? OR CREAT??? OR ELECTROPLAT???
S5 2203771 S SPACER? ? OR BARRIER? ? OR OBSTRUCT???? OR IMPEDIMENT? OR DETERRENT? OR OBSTACLE? ? OR BLOCK???
S6 431544 S CROSSTALK? OR CROSS()TALK? OR NOISE OR INTERFERENCE? ?
S7 195 S S2()S1
S8 28459 S (S4(1W)S3)(50N)S5
S9 0 S S7(S)S8
S10 2 S S7(S)S3(S)S4(S)S5 [not relevant]
S11 72 S S1(S)S3(S)S4(S)S5
S12 8 S S6(S)S11
S13 7 S S12 NOT S10

13/3,K/6
Dialog Global Reporter

29346753 **(USE FORMAT 7 OR 9 FOR FULLTEXT)**
ADVISORY/Cadence Design Systems Presents Demonstrations at DAC Showcasing the Latest Electronic Design Automation Technologies
BUSINESS WIRE
May 27, 2003
Journal Code: WBWE **Language:** English **Record Type:** FULLTEXT
Word Count: 1231
(USE FORMAT 7 OR 9 FOR FULLTEXT)
...learn how to detect a failure and analyze the results, and demonstrate the team design concepts. The demo includes a look at the comparison and **creation** of analog behavioral models (Verilog-A) from transistor design by automatically **creating** a characterization plan. Featured products: Aptivia Circuit Design Environment and Aptivia Design Characterization Modeling (DCM) Physical verification & analysis Customers will see the latest developments in...
...solution to provide "abstract" verification, a new approach that signals new possibilities in addressing physical verification challenges. Featured products: Assura Design Rule Checker (DRC), Assura **Layout** Versus Schematic Verifier (LVS), Assura Parasitic Extractor (RCX) Custom chip authoring This demonstration focuses on the benefits of Virtuoso Chip Editor--the cockpit for chip finishing, featuring OpenAccess infrastructure technology for high-performance and high-capacity interactive editing, abstract swapping, PG text **creation**, layer fill using Assura physical verification. **Blocks** authored in the Virtuoso-XL **layout** environment will be combined with digital **blocks** from the Cadence SoC Encounter environment to **create** a M/S custom IC. Customers will see new connectivity-aware **layout** features that allow precise, manual, geometric editing while assuring design integrity from automatic tools. Pre/post-**route** **creation**, editing with the new wire editor, and top-level MS auto **routing** with Cadence Chip Assembly **Router** will also be shown. Featured products: Virtuoso Chip Editor RTL Compiler - Synthesis for timing closure This demonstration shows the next-generation

optimization technology from Get2Chip...
...learn about the Encounter digital IC design platform and its silicon-proven nanometer sign-off analysis flow covering 3-D extraction, IR drop, timing, and **crosstalk** analysis. The demo includes how to migrate from the Encounter platform to OpenAccess seamlessly for chip finishing and wire editing. Featured products: SoC Encounter RTL-to-GDSII Hierarchical IC Implementation Solution, Fire & Ice(R) QX C Extractor, CeltIC(TM) **Crosstalk** Analyzer, SignalStorm(TM) Signal Integrity Timing Solution, VoltageStorm(TM) SoC Power Grid Verification, Virtuoso Chip Editor SoC Encounter - Hierarchical RTL-to-GDSII solution Cadence SoC...
...tured Product: Virtuoso **Layout** Editor running side-by-side on OpenAccess and CDBA Interconnect design and analysis across silicon-package-board Customers will see how SPECCTRAQuest(R) ST expert can be used for the exploration, **design**, optimization and implementation of multigigabit interconnect from IC die through IC package onto the **PCB**. SPECCTRAQuest offers a single integrated pre- and post-**route design** solution for SI/**crosstalk** and power integrity. This is the only solution that enables the optimization of the interconnect from I/O cell to I/O cell across the fabrics of silicon, IC package and **PCB**. Featured products: SPECCTRAQuest SI expert High-speed constraint-driven **PCB** Design Today's **PCB** systems designers face the incredible challenge of managing design performance from IC die to IC die. Designers must manage timing **paths** and budgets across multiple fabrics concurrently in order to meet system performance goals. This demo shows why most systems companies today use a Cadence **PCB** design flow, the industries only high-speed constraint driven silicon-package-board solution. Featured products: Concept(R) HDL, Allegro(R) **PCB Layout**, SPECCTRA(R) **Router**, SPECCTRAQuest high-speed **PCB** design and analysis, Constraint Manager(TM) IC Package design and analysis The Cadence IC Packaging solution provides an advanced environment for the complete design and...
...in package (SiP). Customers will see how it offers the industry's most robust set of capabilities by providing the framework for IC integration, physical **layout**, package modeling, interconnect **routing**, and analysis which are all key in developing an optimized IC device. Featured products: Advanced Package Designer, Advanced Package Engineer (includes SPECCTRAQuest for IC Packaging...

13/3,K/7
Dialog Global Reporter

18668702 (USE FORMAT 7 OR 9 FOR FULLTEXT)
PCB Design Conference East to Showcase Latest in Printed Circuit Board Design Tools
PR NEWSWIRE
September 05, 2001
Journal Code: WPRW Language: English Record Type: FULLTEXT
Word Count: 730
...a complete pre-route signal integrity toolset; FabFactory, the latest addition to its suite of manufacturing solutions; HyperLynx, a pre and post route signal integrity, cross-talk and EMC toolset; Power PCB, a Windows-based tool for design; QUIET, a system level EMI simulator; QUIET Expert, which assesses PCB for electromagnetic compatibility (EMC); and XTK for signal integrity results. * Mentor Graphics Corporation will highlight the Expedition Series' latest release (WG2000.5), featuring a place and route environment, powered by AutoActive technology. * OHIO Design Automation will introduce Harmony, an

add-in package for the Cadence Allegro PCB CAD system; and InterComm 3.5 with the ability to flip and rotate an entire PCB design. * Polar Instruments will showcase Si6000b, a field solving controlled impedance PCB design system. * Precience Inc. will highlight PCBNavigator 3.1 with bi-directional integration between schematic editors such as OrCAD and PCB systems such as PADS at the database level. * T-Tech, Inc. will introduce Quick Circuit Z-Air, a new circuit board prototyping system. * Valor will highlight Enterprise 3000, DFm software for OEMs and PCB designers that offers a virtual manufacturing system to simulate the entire production process, from design to manufacture to assembly, concurrently with the design process; and... ...Parts Library, a fully integratable online SQL based component/ package library service. * Zuken USA will showcase CADSTAR, a desktop, Windows-based integrated schematic capture through PCB design solution; and VISULA6, a workstation, multi platform, advanced PCB and MCM layout tool. About PCB Design Conference East

[File 350] **Derwent WPIX** 1963-2007/UD=200777

[File 347] **JAPIO** Dec 1976-2007/Jun(Updated 070926)

[File 344] **Chinese Patents Abs** Jan 1985-2006/Jan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Set     Items   Description
S1     283274   S PCB OR PCBS OR CIRCUIT()BOARD? ? OR CIRCUITBOARD? ? OR (PC OR CPU OR
C()P()U OR MOTHER)()BOARD? ? OR MOTHERBOARD? ? OR CIRCUIT()CARD? ? OR PRINTED()CIRCUIT? ?
S2     512590   S VIRTUAL OR DESIGN
S3    1192624   S TRACE OR TRACES OR PATH? ? OR PATHWAY? ? OR TRACK? ? OR CIRCUITPATH? OR
ROUTE OR ROUTES OR TRAIL? ?
S4    1811044   S ROUT??? OR LAY???()OUT OR LAYOUT? ? OR PRINT??? OR CREAT??? OR
ELECTROPLAT???
S5    2036722   S SPACER? ? OR BARRIER? ? OR OBSTRUCT???? OR IMPEDIMENT? OR DETERRENT? OR
OBSTACLE? ? OR BLOCK???
S6     608316   S CROSSTALK? OR CROSS()TALK? OR NOISE OR INTERFERENCE? ?
S7    1374653   S IC=G06F?
S8        186   S S2()S1
S9       5754   S (S4(1W)S3)(50N)S5
S10         0   S S8 AND S9
S11     18383   S S3(S)S4(S)S5
S12         5   S S8 AND S11
S13       797   S S1 AND S11
S14        98   S S1 AND S9
S15         7   S S6 AND S14
S16        72   S S6 AND S13
S17        12   S S12 OR S15
S18        33   S S1/TI AND S11/TI
S19       112   S S13 AND S7
S20         3   S S18 AND S7
S21         3   S S20 NOT (S12 OR S15)
S22         1   S S18 AND S2
S23         2   S S18 AND S6
S24         3   S S22:S23 NOT (S12 OR S15 OR S20)
S25        27   S S18 NOT (S12 OR S15 OR S20 OR S22 OR S23)
S26   1816399   S IC=G06?
S27         0   S S25 AND S26
```

17/25,K/1 (Item 1 from file: 350)
Derwent WPIX

0016045396 *Drawing available*
WPI Acc no: 2006-577027/200659
XRPX Acc No: N2006-464346
Printed circuit board for use in electronic apparatus, has non-conductive substrate, circuit traces, circuit pads and plated-through holes, where plated through holes are electrically connected to intermediate layers of board
Patent Assignee: TA S H (TASH-I)
Inventor: TA S H
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Update	Type
US 20060172614	A1	20060803	200659	B

Local Applications (no., kind, date): US 200551393 A 20050203
Priority Applications (no., kind, date): US 200551393 A 20050203

Alerting Abstract US A1

NOVELTY - The board has a non-conductive substrate, an upper surface, a lower surface, a set of circuit traces, a set of circuit pads and plated-through holes (4-6). A **trace** terminal (12) is electrically connected to the adjacent hole on a right of the board and is used for a signal input, a signal ground, a supply voltage, and a power ground. The plated through holes are electrically connected to intermediate layers of the board.
DESCRIPTION - An INDEPENDENT CLAIM is also included for a method for interconnecting a combination of universal systems **printed-circuit blocks**.
USE - Used for a universal systems **printed circuit block** (USPCB) in an electronic apparatus.
ADVANTAGE - The board effectively reduces an implementation of the electronic systems down to the systems design, the **printed circuit board** assembly, and systems test. The board effectively creates the universal systems **printed-circuit block** by installing on the systems **printed-circuit board** standard function circuit so that the **block** is used and reused over and over again during any phases of a product cycle.
DESCRIPTION OF DRAWINGS - The drawing shows an enlarged plan view of an upper surface of a common USPCB which comprises a multilayer **printed circuit board** for surface-mounted components.
1 Height
2 Variable width
4-6, 8-10 Plated through holes
12-19 **Trace** terminals

Original Abstracts: ...devices and a system is built from circuits. This invention aims at reducing the implementation of electronic systems down to just three steps namely, systems **design**, **printed-circuit-board** planar assembly, and systems test when-as a plurality of Universal Systems Printed-Circuit Blocks of pre-defined sizes is used. Each of said Universal...

17/25,K/6 (Item 6 from file: 350)
Derwent WPIX

0009011761 *Drawing available*
WPI Acc no: 1998-568011/199848
XRPX Acc No: N1998-441900
Interface module for computer system - includes conductive shields having outboard finger shaped extension contacting conductive barrier and inboard finger shaped extension contacting ground pads on printed circuit board
Patent Assignee: DIGITAL EQUIP CORP (DIGI)
Inventor: BRENCH C E; COE S R; DUNCAN S H; LINDQUIST S E; OLSON R E
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Update	Type
US 5822195	A	19981013	199848	B

Local Applications (no., kind, date): US 1997834793 A 19970331
Priority Applications (no., kind, date): US 1997834793 A 19970331

Alerting Abstract US A
The module (32) comprises a **printed circuit board** having signal **traces** for carrying bus signals between a main circuit area and an expansion area. A connector (42) is provided in an opening formed in a conductive barrier arranged between the main circuit area and the expansion area.
Two conductive shields (52a,52b) having extensions in the form of inboard and outboard fingers (46,48), is arranged adjacent to the connector. The outboard fingers are positioned to contact the conductive **barrier** and the inboard fingers are positioned to contact ground pads (54) on the **printed circuit board**.
ADVANTAGE - Provides high isolation from **noise** and high quality transmission path for databus signals. Permits large number of databus signals to pass between high frequency

processor area and low frequency expansion area. Satisfies electromagnetic emission standards.

Original Abstracts: An interface module for an electronic system that permits signals to pass between a high frequency main **circuit board** area such **as used** for central processing units, memories, or other relatively high clock rate components and a low frequency circuit area such as used for standard peripheral circuit... ... for disk drives, video interfaces and the like. The interconnect module is positioned near an opening in a sheet metal bulkhead used as an electromagnetic **interference** (EMI) barrier around **the** main circuit area. The interface module uses a connector that is surrounded by one or more conductive shields that contain metal fingers on inboard and... ...

Claims: ...bus signals are passed from a main circuit area to an expansion area, the main circuit area being enclosed to reduce the emission of electromagnetic **interference** by **a** conductive **barrier** disposed **between** the main circuit area and the expansion area, the interface module being disposed in an area adjacent an opening formed in the conductive **barrier**, the **interface** module comprising:a printed circuit board having an electrical **ground** plane, and the **printed circuit board** also **having signal traces** formed thereon for carrying the bus signals between the main circuit area and the area adjacent the opening;a connector for carrying the bus signal from the area adjacent the opening to the expansion area, the connector disposed through the opening in the conductive **barrier**; anda conductive shield disposed **adjacent** the connector and extending from an inboard edge to an outboard edge of the connector, the shield having extensions formed on an inboard and outboard... ... the outboard edge positioned to contact the conductive barrier, and the extensions on the inboard edge positioned to contact the electrical ground plane on the **printed circuit board.**

17/3/2 (Item 2 from file: 350)
Derwent WPIX

0015084092 *Drawing available*
WPI Acc no: 2005-433548/200544
Related WPI Acc No: 2003-505429; 2003-513996; 2004-832157; 2005-231380; 2005-433553
XRPX Acc No: N2005-351755
Conductive path routing method in printed circuit board design, involves assigning component pin pair to client computers that are configured to automatically route conductive paths
Patent Assignee: MENTOR GRAPHICS CORP (MENT-N)
Inventor: NATARAJAN V; **PETUNIN V V**; PFEIL C L; SMITH E F; SMITH F E; STARKOV A N; PETUNIN V; PFEIL C; SMITH F; STARKOV A
Patent Family (3 patents, 107 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050114821	A1	20050526	US 2003523697	P	20031121	200544	B
			US 2004870072	A	20040618		
WO 2005052730	A2	20050609	WO 2004US37183	A	20041117	200544	E
EP 1685464	A2	20060802	EP 2004800874	A	20041117	200650	E
			WO 2004US37183	A	20041117		

Priority Applications (no., kind, date): US 2003523697 P 20031121; US 2004870072 A 20040618

17/7/11 (Item 1 from file: 347)
JAPIO

05198437 **Image available**

HIGH FREQUENCY PRINTED CIRCUIT BOARD
Pub. No.: 08-153937 [JP 8153937 A]
Published: June 11, 1996 (19960611)
Inventor: MASUDA NOBORU
Applicant: MURATA MFG CO LTD [000623] (A Japanese Company or Corporation), JP (Japan)
Application No.: 06-294662 [JP 94294662]
Filed: November 29, 1994 (19941129)
ABSTRACT
PURPOSE: To reduce **crosstalk** and mutual **interference** between **circuit** blocks on the same **board**, by forming a plurality of long holes between a plurality of circuit blocks different in function where holes penetrate from a signal line surface of the circuit block to a ground layer, and covering the wall surface with a wall surface conductor layer.
CONSTITUTION: Two elliptical electrodes 5A are arranged between circuit blocks 9A and 9B, and slits 5 are arranged inside the electrodes. A zigzag signal **path** 7 for connecting the circuit blocks is formed between the electrodes 5A. The slits 5 penetrate from the surface of the signal **path** 7, i.e., the mounting surface as far as a rear ground layer G on the board back. The wall surfaces of the slits are covered with wall surface conductor layers W, which are electrically connected with the electrodes 5A. When two slits 5A, 5A are viewed from the board side surface, parts of them overlap in the positional relation, in order that a rectilinear propagation **route** may not be formed between the left side circuit **block** 9A and the right side circuit **block** 9B.

21/25,K/1 (Item 1 from file: 350)
Derwent WPIX

0012632487 *Drawing available*
WPI Acc no: 2002-481392/200252
XRPX Acc No: N2002-380263
Portable electronic apparatus e.g. portable telephone, has spool with top and bottom portions movable between two orientations through different routes due to presence of obstacle in route of PCB arranged between portions
Patent Assignee: KOCH-OSBORNE A (KOCH-I); NOKIA CORP (OYNO); NOKIA MOBILE PHONES LTD (OYNO)
Inventor: KOCH-OSBORNE A
Patent Family (11 patents, 28 countries)

Patent Number	Kind	Date	Update	Type
EP 1198037	A2	20020417	200252	B
GB 2368199	A	20020424	200252	E
US 20020045370	A1	20020418	200252	E
JP 2002196839	A	20020712	200261	E
US 6568947	B2	20030527	200337	E
GB 2401492	A	20041110	200474	E
GB 2368199	B	20050330	200523	E
GB 2401492	B	20050330	200523	E
EP 1198037	B1	20051214	200602	E
DE 60115801	E	20060119	200614	E
DE 60115801	T2	20060810	200654	E

EP 1198037
Local Applications (no., kind, date): EP 2001308611 A 20011009; GB 200025149 A 20001013; US 2001835493 A 20010417 ; JP 2001311664 A 20011009; US 2001835493 A 20010417; GB 200025149 A 20001013; GB 200416025 A 20040719; GB 200025149 A 20001013; GB 200025149 A 20001013; GB 200416025 A 20040719; EP 2001308611 A 20011009; DE 60115801 A 20011009; EP 2001308611 A 20011009; DE 60115801 A 20011009; EP 2001308611 A 20011009
Priority Applications (no., kind, date): GB 200025149 A 20001013; EP 2001308611 A

20011009; GB 200416025 A 20040719

Alerting Abstract EP A2
NOVELTY - Top and bottom portions of a spool in portable electronic apparatus, are relatively movable between two orientations and are electrically connected by a flexible **printed circuit board** connector (300). The **route** of the connector between the two portions, has an **obstacle** such that the connectors follow different **routes** in two different orientations.
USE - E.g. personal organizers, laptop computers and mobile telephone.
ADVANTAGE - The connector provides reliable electrical interconnection. The stress and strain to which the flexible connector is subjected to, are kept at acceptable, determinable levels. The **route** taken by connector is repeatable and predictable and hence the **routing** of the connector through **obstacle** is made in such a way that minimum bend radius is not reached, thereby possible damage to the connector is eliminated.
DESCRIPTION OF DRAWINGS - The figures show the profile views of hinge component in various positions between open and closed positions of portable electronic apparatus.
300 Flexible **printed circuit board** connector

21/25,K/2 (Item 2 from file: 350)
Derwent WPIX

0003965253
WPI Acc no: 1987-057785/198709
Computer aided laying-out procedure for multilayered PCB - providing information on position of blocked conductor route to enable manual adjustments by operator.
Patent Assignee: GENERAL ELECTRIC CO PLC (ENGE)
Inventor: HOSKING K
Patent Family (2 patents, 2 countries)

Patent Number	Kind	Date	Update	Type
DE 3628368	A	19870226	198709	B
GB 2179478	A	19870304	198709	E

DE 3628368
Local Applications (no., kind, date): DE 3628368 A 19860821; GB 198521246 A 19850824
Priority Applications (no., kind, date): GB 198521246 A 19850824

Alerting Abstract DE A
If the computer cannot find a way to place a conductor (31) -either because all the available space is already occupied by previously placed conductors or there is a through hole in the only available route - the proceedure stops. The computer identifies the conductors whose **routes** are already planned in the region in question, which cannot be placed, and the position of the **obstacle**, and brings these to the notice of the operator. The most usual obstacle is a through hole (V6).
With the information provided the operator can move the position of the offending hole to a new location (V6') and instruct the computer to return to the placing process. Alternatively, the operator can complete the blocked **route** manually. For identification purposes the **PCB** is divided up by notional grid lines.
USE - On all PCBs but mainly on multilayer double sided **circuit boards.**

21/25,K/3 (Item 3 from file: 350)
Derwent WPIX

0003821478
WPI Acc no: 1986-275829/198642
Automatic wiring system for printed circuit board - sets artificial obstacle and

determines wiring path to provide short wiring path NoAbstract DWg 0/4
Patent Assignee: HITACHI LTD (HITA); HITACHI SOFTWARE ENGINEE (HITA-N)
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Update	Type
JP 61201496	A	19860906	198642	B

Local Applications (no., kind, date): JP 198541120 A 19850304; JP 198541130 A 19850304
Priority Applications (no., kind, date): JP 198541120 A 19850304

24/25,K/1 (Item 1 from file: 350)
Derwent WPIX

0016500715 *Drawing available*
WPI Acc no: 2007-216941/200722
XRAM Acc no: C2007-079398
XRPX Acc No: N2007-160771
Surface mount grid array e.g. pin grid array, for printed circuit board, has connection blocks with array of pins and array of vias, where pins and vias communicatively connect integrated circuit device to traces of circuit board
Patent Assignee: NVIDIA CORP (NVID-N)
Inventor: THOMAS S A
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Update	Type
US 7161812	B1	20070109	200722	B

Local Applications (no., kind, date): US 2003461462 P 20030408; US 2003442355 A 20030520
Priority Applications (no., kind, date): US 2003461462 P 20030408; US 2003442355 A 20030520

Alerting Abstract US B1
NOVELTY - The array has connection blocks (601-606) with an array of pins and an array of vias. The pins and vias are configured to communicatively connect an **integrated circuit** device to **traces** of a **printed circuit board**. The connection **blocks** are disposed in a tiled arrangement, and implement **trace** escape channels (621-622) along connection block boundaries. The pins along the boundaries are connected to vias toward a center of each respective connection **block**. The **trace** escape channels **route traces** from inside pins (630) of the array to the periphery of the array.
DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
a ball grid array package, comprising trace escape channels for **routing** signal **traces**
a system for implementing optimized **trace** escape **routing** comprising a **printed circuit board** for mounting an integrated circuit device.
USE - Surface mount grid array e.g. ball grid array and pin grid array, for use on **printed circuit board (PCB)** (claimed) that is used for connecting a digital processor integrated circuit device that is used for implementing a complex function such as three dimensional graphics application voice recognition and data visualization, in a computer system.
ADVANTAGE - The array of pins and the array of vias of the connection **blocks** are configured to replace a pin with a via to ensure the tiled arrangement, thus enabling the **trace** escape channels to minimize the impact of the vias on the **trace** escape **routing** of the **printed circuit board (PCB)**, and hence allowing a **trace escape routing** pattern from an integrated circuit device to be implemented with fewer **PCB** layers. The reduction in the number of **PCB** layers reduces the cost and increases the reliability of the resulting PCB. The utilization of the **trace** escape channels provide an added degree of trace escape **route** ability, thus allowing the use of **design** rules and via construction technology for the fabrication of **PCBs**, and eliminating the requirement for exotic or overly expensive **PCB** fabrication technology. The array improves the arrangement of via holes in the copper planes, in the direction of current flow.

DESCRIPTION OF DRAWINGS - The drawing shows a set of connection blocks of a ball grid array package as they implement trace escape channels.
601-606 Connection blocks
621-622 Trace escape channels
630 Inside pins
640 Trace fan out

24/25,K/2 (Item 2 from file: 350)
Derwent WPIX

0016118282 *Drawing available*
WPI Acc no: 2006-649912/200668
XRPX Acc No: N2006-524057
Optical interconnection unit for light curtain or light barrier, has printed circuit board comprising conducting paths, and optical lens integrated in board, where board is rigid and lens is attached to receiving and/or transmitting unit
Patent Assignee: SICK AG (SIOP)
Inventor: BECK M
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Update	Type
DE 102005008885	A1	20060907	200668	B

Local Applications (no., kind, date): DE 102005008885 A 20050226
Priority Applications (no., kind, date): DE 102005008885 A 20050226

Alerting Abstract DE A1
NOVELTY - The unit has a **printed circuit board** (4) consisting of a transparent plastic with conducting **paths**. An optical receiving and/or transmitting unit is fastened to the **paths** and sends and receives light within infrared region. A light entry side and/or a light exit side of the unit are positioned in the direction of the board. The board is rigid and an optical lens (14) is integrated in the board, where the lens is attached to the unit.
DESCRIPTION - An INDEPENDENT CLAIM is also included for an application of an optical interconnection unit.
USE - Used for a light curtain or light **barrier** (Claimed) that is utilized for a lighting unit e.g. stroboscope lamp and neon lamp lighting, and a light sensor in an electronic industry.
ADVANTAGE - The **printed circuit board** is rigid and the optical lens is integrated in the board, such that no connection points present between the lens and the board, thus eliminating the need for aligning the lens at the receiving and/or transmitting unit, and hence avoiding disturbing **interferences** of light at junction points. The board consisting of the transparent plastic with the optical lens is used directly as face-plate of the light curtain, thus avoiding the need for additional components and optical interfaces, and hence preventing the light from being refracted unnecessarily at the interfaces and reducing the costs of the face-plate. The interconnection unit allows the light curtain to be integrated in small machines in electronic industry in a simple and versatile manner. The receiving and transmitting unit receives and sends light within the infrared region, thus facilitating the light curtain to be insensitive in relation to foreign light influences from the environment e.g. stroboscope lamps and neon tube lamp, and hence increasing the availability and security of the light curtain.
DESCRIPTION OF DRAWINGS - The drawing shows a schematic representation of an optical interconnection unit.
4 Printed circuit board
8 Electronic component
10 Optical receiving and/or transmitting unit
14 Optical lens
20 Conducting paths

24/25,K/3 (Item 3 from file: 350)
Derwent WPIX

0013412884 *Drawing available*
WPI Acc no: 2003-503250/200347
Related WPI Acc No: 2003-138178
XRAM Acc no: C2003-134348
XRPX Acc No: N2003-399488
Printed circuit boards connection apparatus for computer systems, includes spacer block between two printed circuit boards, through which insulated conductive paths are passed to provide signal integrity
Patent Assignee: BASHAM E (BASH-I); SHAEFFER I P (SHAE-I)
Inventor: BASHAM E; SHAEFFER I P
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Update	Type
US 20030014728	A1	20030116	200347	B

Local Applications (no., kind, date): US 2000561808 A 20000429; US 2002243432 A 20020913
Priority Applications (no., kind, date): US 2000561808 A 20000429; US 2002243432 A 20020913

Alerting Abstract US A1
NOVELTY - A **spacer block separates two printed circuit boards** (PCB1, PCB2), to prevent **interference** between their surface mounted components. The surfaces of the **spacer block**, are electrically connected to the boards, respectively. Conductive **paths** through the spacer block, are insulated to provide high signal integrity for communication between the boards.
DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
printed circuit boards connection provision method; and
compact printed circuit boards connection provision system.
USE - For PCBs used in computer systems.
ADVANTAGE - Provides robust mechanical and electrical connection between two or more PCBs, with greater communication signal integrity.
DESCRIPTION OF DRAWINGS - The figure shows an illustration of an ASIC and a pedestal, on the same PCB.
PCB1, PCB2 Printed circuit boards

Claims: ...attachment of said **circuit boards**, the apparatus comprising: a **spacer block** dimensioned to provide separation between first and second **printed circuit boards** sufficient to prevent **interference** between surface mount components mounted to said first and second **printed circuit boards**; first and second surfaces of said **spacer block** configured for electrical connection, respectively, to said first and second printed circuit boards; and conductive...

25/25,K/1 (Item 1 from file: 350)
Derwent WPIX

0016894221 *Drawing available*
WPI Acc no: 2007-609283/200758
XRPX Acc No: N2007-473675
Pattern drawing apparatus for formation of circuit pattern on photoresist film of printed circuit board, has optical path length adjustment unit changing length of optical path between irradiated block and light emission pixel
Patent Assignee: SUMITOMO HEAVY IND LTD (SUMH)
Inventor: KOBAYASHI K

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Update	Type
JP 2007206176	A	20070816	200758	B

Local Applications (no., kind, date): JP 200622515 A 20060131
Priority Applications (no., kind, date): JP 200622515 A 20060131

Alerting Abstract JP A .
NOVELTY - The pattern drawing apparatus has an optical **path** length adjustment unit for changing the length of an optical **path** between an irradiated **block** (20) and a light emission pixel of a light emission pixel array (2) radiating pencils of rays. The optical path length adjustment unit has a reflection mirror array (7) reflecting the pencils of rays radiated from the light emission pixels and a reflective mirror drive mechanism (6) for displacing the reflective mirrors in a direction parallel to the propagation direction of the pencils of rays.
DESCRIPTION - An INDEPENDENT CLAIM is included for pattern drawing method.
USE - For formation of circuit pattern on photoresist film of **printed circuit board**.
ADVANTAGE - The pencils of rays are made to enter in the irradiated block even when the height of the surface of the irradiated block is not constant by changing the optical path length of the pencils of rays radiated from the light emission pixel.
DESCRIPTION OF DRAWINGS - The figure shows the top and front views of the pattern drawing apparatus.
1 Drive circuit
2 Light emission pixel array
6 Reflective mirror drive mechanism
7 Reflective mirror array
20 Irradiated block

25/25,K/2 (Item 2 from file: 350)
Derwent WPIX

0016567021 *Drawing available*
WPI Acc no: 2007-281959/200727
XRAM Acc no: C2007-103172
XRPX Acc No: N2007-208196
Electronic device has spacer element with one surface contacts printed circuit board and another surface contacts gasket, where conducting paths of surfaces couples to conductive path of shielding element and printed circuit board
Patent Assignee: DUDAS E (DUDA-I); WALLACE P J (WALL-I)
Inventor: DUDAS E; WALLACE P J
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Update	Type
US 20070035939	A1	20070215	200727	B

Local Applications (no., kind, date): US 2005204592 A 20050815
Priority Applications (no., kind, date): US 2005204592 A 20050815

Alerting Abstract US A1
NOVELTY - The device has a shielding element for shielding the electronic components arranged in the **printed circuit board** (PCB) (260) from the electrical signals. An elastomeric gasket (220) forms an electrically conductive **path** between the shielding element and the contacting surface (230) of the gasket. A **spacer** element with one surface contacts the **printed circuit board** and another surface contacts the surface of the gasket, where the conducting **path** of the two surfaces couples to the conductive path of the shielding element and PCB.
DESCRIPTION - An INDEPENDENT CLAIM is included for electronic device manufacturing method.

USE - For electronic device.
ADVANTAGE - The longevity and efficiency of the electrical connection between the **PCB** and other components are significantly improved because of the highly connective and corrosion resistant nature of the interface. A lower cost coating with a lower conductivity such as organic solder preservative (OSP) is used since the coating is not necessary for electrical coupling therefore the manufacturing cost is decreased.
DESCRIPTION OF DRAWINGS - The figure shows an electrical contact point coupling system.
220 Elastomeric gasket
230 Contact surface
240 Interface
250 Solder
260 Printed circuit board

25/25,K/7 (Item 7 from file: 350)
Derwent WPIX

0014853931 *Drawing available*
WPI Acc no: 2005-201635/200521
Related WPI Acc No: 2006-754725; 2006-755103
XRAM Acc no: C2005-064277
XRPX Acc No: N2005-165962
Semiconductor package substrate, e.g. printed circuit board and integrated circuit package substrate, includes insulating layer(s) having conductive blind vias, patterned trace layer(s) comprising contact pads, and metal barrier layer(s)
Patent Assignee: HSU S (HSUS-I); QUANMAO PRECISION SCI & TECHNOLOGY CO LT (QUAN-N); TSAI K (TSAI-I); PHOENIX PRECISION TECHNOLOGY CORP (PHOE-N)
Inventor: HSU S; TSAI K
Patent Family (3 patents, 2 countries)

Patent Number	Kind	Date	Update	Type
US 20050037601	A1	20050217	200521	B
JP 2005064498	A	20050310	200521	E
US 7081402	B2	20060725	200649	E

US 20050037601
Local Applications (no., kind, date): US 2003695356 A 20031027; JP 2004227056 A 20040803; US 2003695356 A 20031027
Priority Applications (no., kind, date): TW 2003122202 A 20030813; US 2003695356 A 20031027

Alerting Abstract US A1
NOVELTY - A semiconductor package substrate having a contact pad protective layer comprises an insulating layer(s) having conductive blind vias and electrically connected to inner **traces** disposed underneath the insulating layer, a patterned **trace** layer(s) electroplated via a conductive film on the insulating layer and comprising contact pads (64) electrically connected to the blind vias, and a metal **barrier** layer(s) (65) for covering the contact pads.
DESCRIPTION - An INDEPENDENT CLAIM is also included for a method for fabricating a semiconductor package substrate having a contact pad protective layer, comprising:
providing an insulating layer having blind vias for exposing inner traces disposed underneath the insulating layer;
forming a conductive film on the insulating layer and over the blind vias;
forming a first resist layer on the conductive film, having openings to expose predetermined parts of the conductive film;
performing a first electroplating process to form a patterned **trace** layer in the openings and in the blind vias to form conductive vias, where the patterned **trace** layer comprises contact pads electrically connected to at least one of the conductive vias;

forming a second resist layer over the patterned **trace** layer exclusive of the contact pads, making the contact pads exposed from the second resist layer;
performing a second **electroplating** process to form a metal barrier layer on the contact pads; and
removing the second resist layer, the first resist layer, and parts of the conductive film covered by the first resist layer.
USE - The invention is used as, e.g. **printed circuit board** and **integrated circuit** package substrate for flip-chip package (60).
ADVANTAGE - The invention prevents corrosive attack of solder mask and solder mask peeling.
DESCRIPTION OF DRAWINGS - The figure shows a schematic, cross-sectional view of a flip-chip package.
60Flip-chip package
62Chip
63Metal bumps
64Contact pads
65Metal barrier layer

25/25,K/16 (Item 16 from file: 350)
Derwent WPIX

0012658125 *Drawing available*
WPI Acc no: 2002-507868/200254
XRPX Acc No: N2002-401944
A low-inductance connection for components on a printed circuit board includes a conducting path on a second printed circuit board separated by spacers and an insulating gas, and an electrical connector to a first conducting path
Patent Assignee: AMERICAN SUPERCONDUCTOR CORP (AMSU-N)
Inventor: REICHARD J A
Patent Family (3 patents, 95 countries)

Patent Number	Kind	Date	Update	Type
WO 2002028155	A1	20020404	200254	B
AU 200191249	A	20020408	200254	E
US 6472613	B1	20021029	200274	E

WO 2002028155
Local Applications (no., kind, date): WO 2001US30068 A 20010926; AU 200191249 A 20010926; US 2000677097 A 20000929
Priority Applications (no., kind, date): US 2000677097 A 20000929

Alerting Abstract WO A1
NOVELTY - A component (18) has a first conducting **path** (26) to a second component on a top surface (14) of a **printed circuit board** (12). A low-inductance connection includes a second conducting **path** (32) disposed on a surface (30) of a second **printed circuit board** (28) separated by **spacers** (42) and supports (44) and having an insulating gas layer (38). An electrical connector (40) provides a connection having a parasitic inductance smaller than that of the first conducting **path**.
DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
a method for electrically connecting components on a printed circuit board
and a power converter.
USE - The low-inductance connection is used for a **printed circuit board**.
ADVANTAGE - Additional area is not required on the printed circuit board so that cost is reduced and circuit board deflection that may weaken component connections is minimized.
DESCRIPTION OF DRAWINGS - The figure shows a cross-sectional view of a printed circuit board with a low-inductance connection.
12 Printed circuit board

14 Top surface
18 Component
26 First conducting path
28 Second printed circuit board
30 Surface
32 Second conducting path
38 Insulating gas layer
40 Electrical connector
42 Spacer
44 Support

17/26/3 (Item 3 from file: 350)
Derwent WPIX

0014614059 *Drawing available*
WPI Acc no: 2004-796032/200478
Electronic component mounting apparatus stores position and height of obstruction with respect to extracting/mounting height of components based on which nozzle moving unit or raising/lowering unit is controlled

17/26/5 (Item 5 from file: 350)
Derwent WPIX

0011036338 *Drawing available*
WPI Acc no: 2001-662414/200176
Testing method of circuit on printed circuit board, involves creating new test point by depositing procoat on surface of printed circuit board excepting on identified access point

17/26/8 (Item 8 from file: 350)
Derwent WPIX

0008053300 *Drawing available*
WPI Acc no: 1997-148164/199714
Switching unit especially for aircraft entertainment system - has crosspoint unit which establishes several paths between input and output and has router which selects path, via crosspoint unit, for distributing signals

17/26/9 (Item 9 from file: 350)
Derwent WPIX

0007848717 *Drawing available*
WPI Acc no: 1996-478589/199648
Electrically operated window circuit board overcurrent protection appts. for vehicle - limits current in trace using polyswitch resettable fuse between power source and circuit board

17/26/10 (Item 10 from file: 350)
Derwent WPIX

0006700088 *Drawing available*
WPI Acc no: 1994-080638/199410
Radio frequency earthing switch for magnetic resonance imager - uses PCB and includes variable tuning capacitor

17/26/12 (Item 2 from file: 347)

JAPIO

03871571 **Image available**
AUTOMATIC PEELING/REWIRING METHOD

25/26/3 (Item 3 from file: 350)
Derwent WPIX

0016114958 *Drawing available*
WPI Acc no: 2006-646587/200667
Multi-chip module for e.g. micro computer, has optical path converting block inserted into inserting hole formed on printed circuit board so as to intersect optical guide when mounting multi-chip module

25/26/4 (Item 4 from file: 350)
Derwent WPIX

0016059182 *Drawing available*
WPI Acc no: 2006-590813/200661
Foreign material removal jig for printed wiring board has spacer portion connecting with gas introduction opening and suction apparatus opening and forms gas flow path between circuit board of printed wiring board

25/26/5 (Item 5 from file: 350)
Derwent WPIX

0015522443
WPI Acc no: 2006-086591/200609
Heat-activable adhesive tape for bonding electronic components and conductor tracks, e.g. flexible printed circuit boards, comprises adhesive with acid modified or acid-anhydride-modified vinyl aromatic block copolymer, and epoxide compound

25/26/6 (Item 6 from file: 350)
Derwent WPIX

0015170279 *Drawing available*
WPI Acc no: 2005-519862/200553
Spacer post for fastening printed circuit board of LCD device, has upper end face to abut against upper circuit layer and formed with inner threaded hole, and threaded lower portion for fastening to base via threaded hole of lower layer

25/26/8 (Item 8 from file: 350)
Derwent WPIX

0014762904 *Drawing available*
WPI Acc no: 2005-110558/200512
Laser exposure apparatus for forming wiring pattern in printed circuit board, has recording medium moving along preset circulating path that is within range in which movement of one stage is not obstructed while image is formed

25/26/9 (Item 9 from file: 350)
Derwent WPIX

0014189211 *Drawing available*
WPI Acc no: 2004-374623/200435
Printed circuit board has differential traces to carry high-speed, e.g. microwave, serial data from functional unit block and crossover on same layer of board while maintaining

constant impedance

25/26/10 (Item 10 from file: 350)
Derwent WPIX

0014158965 *Drawing available*
WPI Acc no: 2004-343952/200432
Automatic mounting apparatus for mounting chip-type electronic component on printed circuit board, has manifold block that is integrally provided on upper side of vacuum valve, which has vacuum-suction and compressed-air blow routes

25/26/11 (Item 11 from file: 350)
Derwent WPIX

0014153504 *Drawing available*
WPI Acc no: 2004-338407/200431
System for enabling electronic devices on printed circuit board to communicate using network protocol, has matching network to interface medium access control blocks of devices on printed circuit board, with trace pair in circuit board

25/26/12 (Item 12 from file: 350)
Derwent WPIX

0014095930 *Drawing available*
WPI Acc no: 2004-279626/200426
Integrated circuit package for high speed digital circuits, has multiple shielding vias which surround signal path and configured for blocking emitted radiation from signal path within printed wiring board

25/26/13 (Item 13 from file: 350)
Derwent WPIX

0013613124 *Drawing available*
WPI Acc no: 2003-708384/200367
Microphone subassembly for telecommunication equipment, has spacer made of flexible printed circuit board that contains exposed metal trace for electrical contact and integral lead portion that transmits signal

25/26/14 (Item 14 from file: 350)
Derwent WPIX

0012938048 *Drawing available*
WPI Acc no: 2003-014668/200301
Signal tracks connection method for multilayered printed circuit board, involves inserting components having dielectric block into opening formed in substrate, to electrically connect signal tracks

25/26/15 (Item 15 from file: 350)
Derwent WPIX

0012913544 *Drawing available*
WPI Acc no: 2002-471608/200250
Ultrasonic transducer array probe for ultrasonic diagnostic imaging system, has conductive backing block assembly with backing block plates and printed circuit substrates with conductive traces which are bonded together

25/26/17 (Item 17 from file: 350)

Derwent WPIX

0009319610 *Drawing available*
WPI Acc no: 1999-251050/199921
Connector press-fitting apparatus for printed circuit board - connects intake path formed in heel block which is mounted to die, to conduction hole formed on die

25/26/18 (Item 18 from file: 350)
Derwent WPIX

0009052737 *Drawing available*
WPI Acc no: 1998-000913/199801
Multilayer substrate for printed circuit board - has inner insulation layer acting as spacer frame with at window being provided for inner electric component, conductive tracks being formed between adjacent insulation layers

25/26/19 (Item 19 from file: 350)
Derwent WPIX

0008818188
WPI Acc no: 1998-363848/199832
Production of electronic printed circuit boards for SMD components - is coated with a protective insulation lacquer with solder blocking lacquer limited to tracks

25/26/20 (Item 20 from file: 350)
Derwent WPIX

0007724620 *Drawing available*
WPI Acc no: 1996-347877/199635
Extension card for functional confirmation test of e.g. electronic circuit - has first block with blower that generates cooling air to opening unit of printed circuit board, and second block which contains flow path discharging cooling air passing through heat sink

25/26/21 (Item 21 from file: 350)
Derwent WPIX

0007311444 *Drawing available*
WPI Acc no: 1995-373331/199548
Probe clamp for testing printed circuit boards - has rotating shaft in base which is coupled to centre block for pivotal movement about axis with drive mechanism for traversing a longitudinal and arcuate path about axis

25/26/22 (Item 22 from file: 350)
Derwent WPIX

0007085943 *Drawing available*
WPI Acc no: 1995-111558/199515
NC course determn method applied to PCB processing by numerical control machine - involves determination of route which passes between location successive blocks computed based on maximum movement distance and minimum mounting cycle time

25/26/23 (Item 23 from file: 350)
Derwent WPIX

0005937657 *Drawing available*
WPI Acc no: 1992-168792/199221

Holographic optical back-plane circuit board interconnector - uses silver halide holographic plate on transparent solid polymeric block to route light beams between light transmitters and receivers on electronic circuit boards

25/26/24 (Item 24 from file: 350)
Derwent WPIX

0005877961 *Drawing available*
WPI Acc no: 1992-105597/199214
Automatic block section module for DC model railway - combines track and signal movement functions on printed circuit board supplied from source of traction voltage

25/26/25 (Item 25 from file: 350)
Derwent WPIX

0004390910 *Drawing available*
WPI Acc no: 1988-126412/198818
Shielding appts. for use in printed circuit board - has circuitry blocks mounted on top surface of PCB and electrically connected by circuit trace

25/26/26 (Item 26 from file: 350)
Derwent WPIX

0004260694
WPI Acc no: 1987-187589/198727
Mfg. wiring in semiconductor IC or PCB - by searching bottle neck in substrate surface while avoiding obstacles, to determine wiring routes. NoAbstract Dwg 3/4

25/26/27 (Item 27 from file: 350)
Derwent WPIX

0001564651
WPI Acc no: 1978-B6739A/197808
Terminal block using printed circuit element - has box like shell through which cable carrying wire conductor connects to conductive paths